MB37
LCD TV
SERVICE MANUAL

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1. INTRODUCTION

17MB37 Main Board consists of MSTAR concept.(Up to 32") This IC is capable of handling Video processing, Audio processing, Scaling-Display processing, 3D comb filter, OSD and text processing, 8 bit dual LVDS transmitter.
TV supports PAL, SECAM, NTSC colour standards and multiple transmission standards as B/G, D/K, I/I', and L/L' including German and NICAM stereo.

Sound system output is supplying max. 2x8W (10%THD) for stereo 8Ω speakers. This will change according to IC thay is being used.
Supported peripherals are:

1 RF input VHF I, VHF III, UHF @ 75Ohm(Common)
1 Side AV (SVHS, CVBS, HP, R/L_Audio) (Common)
1 SCART sockets(Common)
1 YPbPr (Common)
1 PC input(Optional)
2 HDMI 1.3 input(2 HDMI inputs are common)
1 Stereo audio input for PC(Common)
1 Line out(Common)
1 S/PDIF output(Common)
1 Side S-Video(Optional)
1 Headphone(Common)
1 Common interface(Common)
1 Digital USB or 1 Analog USB + 2 Digital USB(Optional)

2. TUNER

A horizontal mounted and Digital Half-Nim tuner is used in the product, which covers 3 Bands(From 48MHz to 862MHz for COFDM, from 45.25MHz to 863.25MHz for CCIR CH). The tuning is available through the digitally controlled I2C bus (PLL). Below you will find info about the tuner.

2.1. General description of TDTC-G101D:

The Tuner covers 3 Bands(from 48MHz to 862MHz for COFDM, from 45.25MHz to 863.25MHz for CCIR CH). Band selection and Tuning are performed digitally via the I2C bus.

2.2. Features of TDTC-G101D:

- Digital Half-NIM tuner for COFDM
- Covers 3 Bands(From 48MHz to 862MHz for COFDM,
- From 45.25MHz to 863.25MHz for CCIR CH)
- Including IF AGC with SAW Filter
- Bandwidth Switching (7/8 MHz) possible
- DC/DC Converter built in for Tuning Voltage
- Internal(or External) RF AGC, Antenna Power Optional

2.3. Pinning:

PIN NAME	PIN No.	PIN Description
Ant PWR	1	+5V (for Active Antenna), Optional
B1	2	+ 5V (for Loop through & DC-DC)
RF AGC	3	N.C
SCL	4	I^2C Bus for TUNER PLL
SDA	5	I^2C Bus for TUNER PLL
B2	6	+ 5V (for TU & IF AGC AMP)
Vtu T.P	7	N.C
AS	8	PLL IC Address selection
IF AGC Control	9	IF AGC Control
DIF2	10	Total IF Output2
DIF1	11	Total IF Output1
AIF	12	Tuner IF Output

3. AUDIO AMPLIFIER STAGE WITH MAX9736(8-10WATT)

3.1. General Description

The MAX9736A/B Class D amplifiers provide high-performance,thermally efficient amplifier solutions. The MAX9736A delivers 2 x 15W into 8Ω loads, or 1 x 30W into a 4Ω load. The MAX9736B delivers 2 x 6W into 8Ω loads or 1 x 12W into a 4Ω load. These devices are pinfor pin compatible, allowing a single audio design to work across a broad range of platforms, simplifying design efforts, and reducing PCB inventory.

Both devices operate from 8V to 28V and provide a high PSRR, eliminating the need for a regulated power supply. The MAX9736 offers up to 88% efficiency at 12V supply.

Pin-selectable modulation schemes select between filterless modulation and classic PWM modulation.

Filterless modulation allows the MAX9736 to pass CE EMI limits with 1m cables using only a low-cost ferrite bead and capacitor on each output. Classic PWM modulation is optimized for best audio performance when using a full LC filter.

A pin-selectable stereo/mono mode allows stereo operation into 8Ω loads or mono operation into 4Ω loads. In mono mode, the right input op amp becomes available as a spare device, allowing flexibility in system design. Comprehensive click-and-pop reduction circuitry minimizes noise coming into and out of shutdown or mute.

Input op amps allow the user to create summing amplifiers, lowpass or highpass filters, and select an optimal gain. The MAX9736A/B are available in 32-pin TQFN packages and specified over the -40°C to +85°C temperature range.

3.2. Features

Wide 8V to 28V Supply Voltage Range

♦ Spread-Spectrum Modulation Enables Low EMI Solution

♦ Passes CE EMI Limits with Low-Cost Ferrite Bead/Capacitor Filter

♦ Low BOM Cost, Pin-for-Pin Compatible Family

♦ High 67dB PSRR at 1kHz Reduces Supply Cost

♦ 88% Efficiency Eliminates Heatsink

♦ Thermal and Output Current Protection

♦ < 1µA Shutdown Mode

♦ Mute Function

♦ Space-Saving, 7mm x 7mm x 0.8mm, 32-Pin TQFN Package

3.3. Applications

LCD/PDP/CRT Monitors
LCD/PDP/CRT TVs
MP3 Docking Stations
Notebook PCs
PC Speakers
All-in-One PCs

3.4. Absolute Ratings

3.4.1. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AMPLIFIER DC CHARACTERISTICS							
Speaker Supply Voltage Range	PVDD	Inferred from PSRR test		8		28	V
Preamplifier Supply Voltage Range	VS	(Notes 1 and 7)		4.5		5.5	V
Undervoltage Lockout	UVLO				7		V
Quiescent Supply Current	I_{PVDD}	R_L = ∞, V_{REGEN} = 5V, V_{VS} = open	T_A = +25°C		30	45	mA
			T_A = T_{MIN} to T_{MAX}			50	
	I_{VS}	R_L = ∞, V_{REGEN} = 0V, V_{VS} = 5V	T_A = +25°C		14	20	mA
			T_A = T_{MIN} to T_{MAX}			22	
Shutdown Supply Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0V	I_{PVDD}		1	10	µA
			I_{VS}			10	
REG Voltage	V_{REG}				4.2		V
Preregulator Voltage	VS	Internal regulated 5V, V_{REGEN} = 5V			4.8		V
COM Voltage	V_{COM}			1.9	2.05	2.2	V
INPUT AMPLIFIER CHARACTERISTICS							
Capacitive Drive	C_L				30		pF
Output Swing (Note 6)		Sinking ±1mA			±2		V
Open-Loop Gain	A_{VO}	$V_{FB\_}$ = V_{COM} ±500mV, $R_{FB\_}$ = 20kΩ to IN_			88		dB
Input Offset Voltage	V_{OS}				±1		mV

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Input Amplifier Slew Rate						2.5		V/µs
Input Amplifier Unity-Gain Bandwidth						3.5		MHz
AMPLIFIER CHARACTERISTICS								
Output Amplifier Gain (Note 8)	A_V	MAX9736A			16.5	17	17.5	dB
		MAX9736B			13.1	13.6	14.1	
Output Current Limit					3.3	4.6		A
Output Offset	V_{OS}	OUT_+ to OUT_-, T_A = +25°C				±2	±10	mV
Power-Supply Rejection Ratio	PSRR	PVDD = 8V to 28V, T_A = +25°C			65	80		dB
		f = 1kHz, 100mV_{P-P} ripple				67		
MAX9736A Output Power (THD+N = 1%)	$P_{OUT\_1\%}$	PVDD = 12V	Stereo	R_L = 8Ω		8		W
				R_L = 4Ω		13		
			Mono	R_L = 4Ω		15.5		
		PVDD = 18V	Stereo	R_L = 8Ω		13.5		
			Mono	R_L = 4Ω		27		
		PVDD = 24V	Stereo	R_L = 8Ω		13.5		
			Mono	R_L = 4Ω		27		
MAX9736B Output Power (THD+N = 1%)	$P_{OUT\_1\%}$	PVDD = 12V	Stereo	R_L = 8Ω		6		W
				R_L = 4Ω		11		
			Mono	R_L = 4Ω		12		
		PVDD = 18V	Stereo	R_L = 8Ω		6		
			Mono	R_L = 4Ω		12		
		PVDD = 24V	Stereo	R_L = 8Ω		6		
			Mono	R_L = 4Ω		12		
MAX9736A Output Power (THD+N = 10%)	$P_{OUT\_10\%}$	PVDD = 12V	Stereo	R_L = 8Ω		10		W
				R_L = 4Ω		16		
			Mono	R_L = 4Ω		19.5		
		PVDD = 18V	Stereo	R_L = 8Ω		17.5		
			Mono	R_L = 4Ω		35		
		PVDD = 24V	Stereo	R_L = 8Ω		17.5		
			Mono	R_L = 4Ω		35		
MAX9736B Output Power (THD+N = 10%)	$P_{OUT\_10\%}$	PVDD = 12V	Stereo	R_L = 8Ω		7.5		W
				R_L = 4Ω		14		
			Mono	R_L = 4Ω		15		
		PVDD = 18V	Stereo	R_L = 8Ω		7.5		
			Mono	R_L = 4Ω		15		
		PVDD = 24V	Stereo	R_L = 8Ω		7.5		
			Mono	R_L = 4Ω		15		

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Harmonic Distortion Plus Noise	THD+N	MAX9736A, P_{OUT} = 4W, f = 1kHz, PWM modulation mode, R_L = 8Ω			0.04		%
		MAX9736B, P_{OUT} = 2W, f = 1kHz, PWM modulation mode, R_L = 8Ω			0.04		
Signal-to-Noise Ratio	SNR	A-weighted	MAX9736A, P_{OUT} = 8W, R_L = 8Ω		96.5		dB
			MAX9736B, P_{OUT} = 6W, R_L = 8Ω		97		
Noise	V_N	A-weighted (Note 9)	MAX9736A		120		μV_{RMS}
			MAX9736B		100		
Crosstalk		L to R, R to L, P_{OUT} = 1W, f = 1kHz, R_L = 8Ω			100		dB
Efficiency	η	P_{OUT} = 8W, MAX9736A, PVDD = 12V, R_L = 8Ω			88		%
Click-and-Pop Level	K_{CP}	Peak voltage, 32 samples/second, A-weighted (Notes 9 and 10)	Into mute		36		dBV
			Out of mute		36		
Switching Frequency				270	300	330	kHz
Spread-Spectrum Bandwidth					±4		kHz
Thermal Shutdown Level					160		°C
Thermal Shutdown Hysteresis					30		°C
Turn-On Time	t_{ON}				110		ms
DIGITAL INTERFACE							
Input Voltage High	V_{INH}			2			V
Input Voltage Low	V_{INL}					0.8	V
Input Voltage Hysteresis					50		mV
Input Leakage Current						±10	µA

3.4.2. Operating Specifications

Parameters	Symbol	Condition	Min	Typ	Max	Units
Standby Current		V_{EN} = 0V		260		µA
Quiescent Current				23		mA
Power Output		f = 1KHz, THD+N = 10%, 4Ω Load		20		W
		f = 1KHz, THD+N = 10%, 8Ω Load		10		W
THD+ Noise		P_{OUT} = 1W, f = 1KHz, 4Ω Load		0.16		%
		P_{OUT} = 1W, f = 1KHz, 8Ω Load		0.06		%
Efficiency		f = 1KHz, P_{OUT} = 1W, 4Ω Load		90		%
		f = 1KHz, P_{OUT} = 1W, 8Ω Load		95		%
Maximum Power Bandwidth				20		KHz
Dynamic Range				93		dB
Noise Floor		A-Weighted		190		µV
Power Supply Rejection		f = 1KHz		60		dB

3.5. Pinning

PIN	NAME	FUNCTION
1, 2	OUTL-	Left-Channel Negative Speaker Output
3	BOOT	Charge-Pump Output. Connect a 1µF charge-pump holding capacitor from BOOT to PGND.
4	MONO	Mono Select. Set MONO high for mono mode, low for stereo mode.
5	FBL	Left-Channel Feedback. Connect feedback resistor between FBL and INL to set amplifier gain.
6	INL	Stereo Left-Channel Inverting Input. In mono mode, INL is the inverting audio input for the mono amplifier.
7, 8, 17	N.C.	No Connection. Not internally connected. OK to connect to PGND.
9	$\overline{\text{MUTE}}$	Mute Input. Drive $\overline{\text{MUTE}}$ low to place the device in mute mode.
10	$\overline{\text{SHDN}}$	Shutdown Input. Drive $\overline{\text{SHDN}}$ low to place the device in shutdown mode.
11	REGEN	Internal Regulator Enable Input. Connect REGEN to $\overline{\text{SHDN}}$ to enable the internal regulator. Drive REGEN low to disable the internal regulator, and supply the device with an external 5V supply on VS. See the *Power-Supply Sequencing* section.
12	COM	Internal 2V Bias. Bypass COM to AGND with a 1µF capacitor.
13, 14	AGND	Analog Ground
15	REG	Internal Regulator Output. Bypass REG to AGND with a 1µF capacitor.
16	VS	5V Regulator Supply. Bypass VS to AGND with a 1µF capacitor. If REGEN is low, the internal regulator is disabled, and an external 5V supply must be connected to VS. See the *Power-Supply Sequencing* section.
18	INR	Stereo Right-Channel Inverting Audio Input. In mono mode, INR is the inverting audio input for the uncommitted preamplifier (see the *Mono Configuration* section for more details).
19	FBR	Right-Channel Feedback. Connect feedback resistor between FBR and INR to set amplifier gain.
20	MOD	Output Modulation Select. Sets the output modulation scheme: V_{MOD} = Low, classic PWM/fixed-frequency mode V_{MOD} = High, filterless modulation/spread-spectrum mode
21	C1N	Charge-Pump Flying-Capacitor Negative Terminal
22	C1P	Charge-Pump Flying-Capacitor Positive Terminal
23, 24	OUTR-	Right-Channel Negative Speaker Output
25, 26	OUTR+	Right-Channel Positive Speaker Output
27, 30	PVDD	Power Supply. Bypass each PVDD pin to ground with 0.1µF capacitors. Also, use a single 220µF capacitor between PVDD and PGND.
28, 29	PGND	Power Ground
31, 32	OUTL+	Left-Channel Positive Speaker Output
—	EP	Exposed Pad. Must be externally connected to PGND.

AUDIO AMPLIFIER STAGE WITH PT2333(2.5 WATT)

The PT2333 is a Class-D power amplifier designed for audio equipments, maximum output power can reach up to 2.5W (VDD=5V, RL=4Ω, THD=10%). The PT2333 composed of exclusively designed Class-D circuitry (patented) by PTC, along with the most advanced semi-conductor technology. When compared to the traditional Class-AB amplifiers, the PT2333's has a much higher efficiency (>80%), low heat dissipation, and produces superior audio quality. PT2333's external circuitry is simple and easily accessible, and consists of flawless self-protection capabilities. The chip's packaging is small, thus it occupies an insignificant amount of space on the circuit board; therefore, making it the predominant choice when it comes to audio amplifiers.

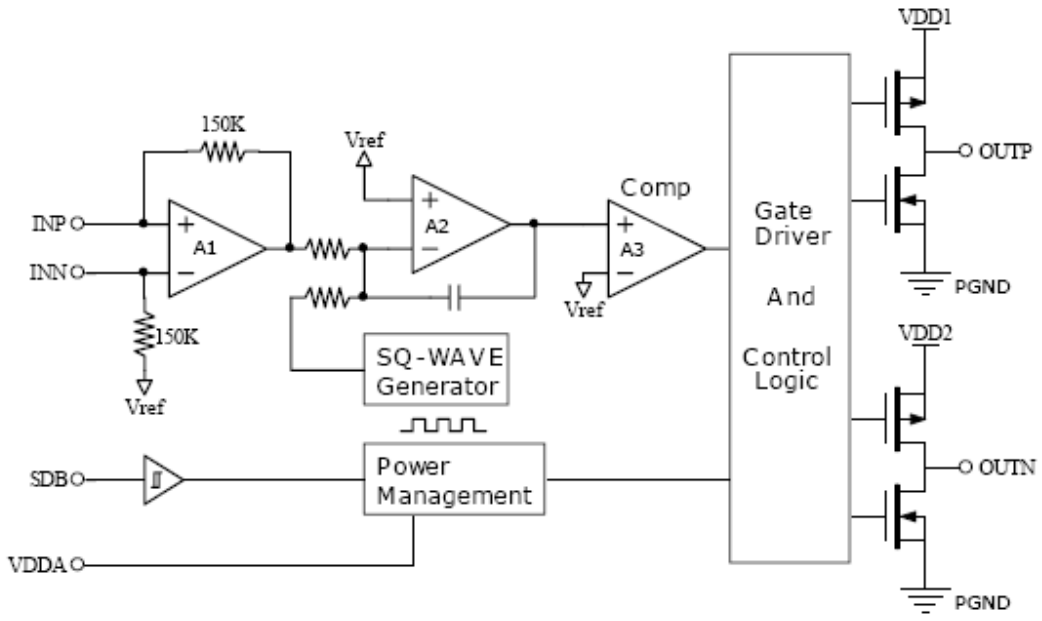
Features

 CMOS technology
 Operating voltage range from 2.7V up to 5.5V
 Differential analog input
 Maximum output power 2.5W(4Ω) @ THD=10%
 Output low-pass LC filter is not required.
 Voltage gain determinate by the external resister
 Contains shutdown function
 POP noises free in shutdown and power ON/OFF period
 Built-in short circuit protection
 Built-in overheat protection
 High efficiency (8Ω load >85%), low heat dissipation
 Available in MSOP 10-pin and WLCSP 9-pin miniature packages

Aplications

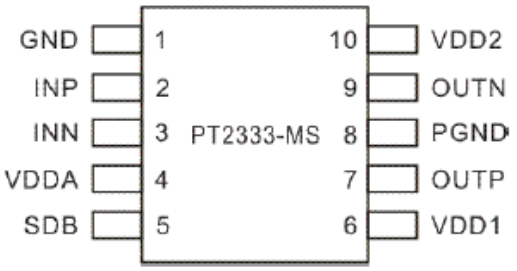
 Cellular phone
 Portable media player
 GPS
 LCD monitor
 Small multimedia speakers
 Hand-free phone
 Laptop
 Other audio applications

Block Diagram



PT2333 Internal Block Diagram

MSOP-10 PACKAGE



Pin	I/O	Symbol	Description	Pin	I/O	Symbol	Description
1	Power	GND	Signal ground	6	Power	VDD1	Power input 1
2	I	INP	Positive input	7	O	OUTP	Positive output
3	I	INN	Negative input	8	Power	PGND	Power ground
4	Power	VDDA	Power input	9	O	OUTN	Negative output
5	I	SDB	Shutdown	10	Power	VDD2	Power input 2

POWER SUPPLY

The operating voltage for the PT2333 is from 2.5V to 6V, and there are several power input pins are VDDA, VDD1, and VDD2 (VDD2 is not presents in WCSP-9 package). In normal operations tight these pin together and at least 1μF bypass capacitor is necessary.

To prevent pop noises be heard during power or shutdown ON/OFF period, PT2333 built-in a under voltage detection circuit; If supply voltage constant exceeds 2.6V, the IC would temporarily go into mute state and next starts working; otherwise the IC will remain in the muted state. If the voltage drops below 2.5V during normal operation, the IC will be quickly muted to prevent pop noises happens.

4. POWER STAGE

The DC voltages required at various parts of the chassis and inverters are provided by a main power supply unit. The power supply generates 33V, 24V, 12V, 5V, 3,3V and 5V, 3,3V stand by mode DC voltages. Power stage which is on-chasis generates 1,26V stand by voltage and 8V, 2.5V, 2,6V, 1,8V and 1V supplies for other different parts of the chassis.

ADAPTOR USE (Optional)

The DC voltages required at various parts of the chassis and inverters are provided by an external power supply unit or produced on the chassis if an adapter is used for the supply. The 12V dc voltage is switched by IRF 7314 power mosfet in TV sets with mechanical switch to produce the required standby voltage. Also regulators and mosfets generate 1.8V, 3.3V and 5V and 1.26V voltages for other different parts of the chassis.

5. MICROCONTROLLER (MSTAR)

Genaral Description

The MST6WB7GQ-3 is a high performance and fully integrated IC for multi-function LCD monitor/TV with resolutions up to full HD (1920x1080). It is configured with an integrated triple-ADC/PLL, an integrated DVI/HDCP/HDMI receiver, a multi-standard TV video and audio decoder, two video de-interlacers, two scaling engines, the MStarACE-3 color engine, an on-screen display controller, an 8-bit MCU and a built-in output panel interface. By use of external frame buffer, PIP/POP is provided for multimedia applications. Furthermore, 3-D video decoding and processing are fulfilled for high-quality TV applications. To further reduce system costs, the MST6WB7GQ-3 also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

5.1. Features

LCD TV controller with PIP/POP display functions

- Input supports up to UXGA & 1080P
- Panel supports up to full HD (1920x1080)
- TV decoder with 3-D comb filter
- Multi-standard TV sound demodulator and decoder
- 10-bit triple-ADC for TV and RGB/YPbPr
- 10-bit video data processing
- Integrated DVI/HDCP/HDMI compliant receiver
- High-quality dual scaling engines & dual 3-D video de-interlacers
- 3-D video noise reduction
- Full function PIP/PBP/POP
- MStarACE-3 picture/color processing engine
- Embedded On-Screen Display (OSD) controler engine
- Built-in MCU supports PWM & GPIO
- Built-in dual-link 8/10-bit LVDS transmitter
- 5-volt tolerant inputs
- Low EMI and power saving features
- 296-pin LQFP

NTSC/PAL/SECAM Video Decoder

- Supports NTSC M, NTSC-J, NTSC-4.43, PAL (B,D,G,H,M,N,I,Nc), and SECAM
- Automatic TV standard detection
- Motion adaptive 3-D comb filter for NTSC/PAL
- 8 configurable CVBS & Y/C S-video inputs
- Supports Teletext level-1.5, WSS, VPS, Closed-caption, and V-chip
- Macrovision detection
- CVBS video output

Video IF for Multi-Standard Analog TV

- Digital low IF architecture
- Stepped-gain PGA with 26 dB tuning range and 1 dB tuning resolution
- Maximum IF analog gain of 37dB in addition to digital gain
- Programmable TOP to accommodate different tuner gain to optimize noise and linearity performance

Multi-Standard TV Sound Decoder

- Supports BTSC/NICAM/A2/EIA-J demodulation and decoding
- FM stereo & SAP demodulation
- L/Rx4, mono, and SIF audio inputs
- L/Rx3 loudspeaker and line outputs
- Supports sub-woofer output
- Built-in audio output DAC's
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, and virtual stereo/surround
- Optional advanced surround available (Dolby1, SRS2, BBE3… etc)

Digital Audio Interface

- I2S digital audio input & output
- S/PDIF digital audio input & output
- HDMI audio channel processing capability
- Programmable delay for audio/video synchronization

Analog RGB Compliant Input Ports

- Three analog ports support up to UXGA
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG (Sync-on-Green) separator
- Automatic color calibration

DVI/HDCP/HDMI Compliant Input Port

- Two HDMI input ports with built-in switch
- Supports TMDS clock up to 225MHz @ 1080P 60Hz with 12-bit deep-color resolution
- Single link on-chip DVI 1.0 compliant receiver
- High-bandwidth Digital Content Protection(HDCP) 1.1 compliant receiver

6. MPEG-2/MPEG-4 DVB Decoder (STi7101)

6.1. General Description

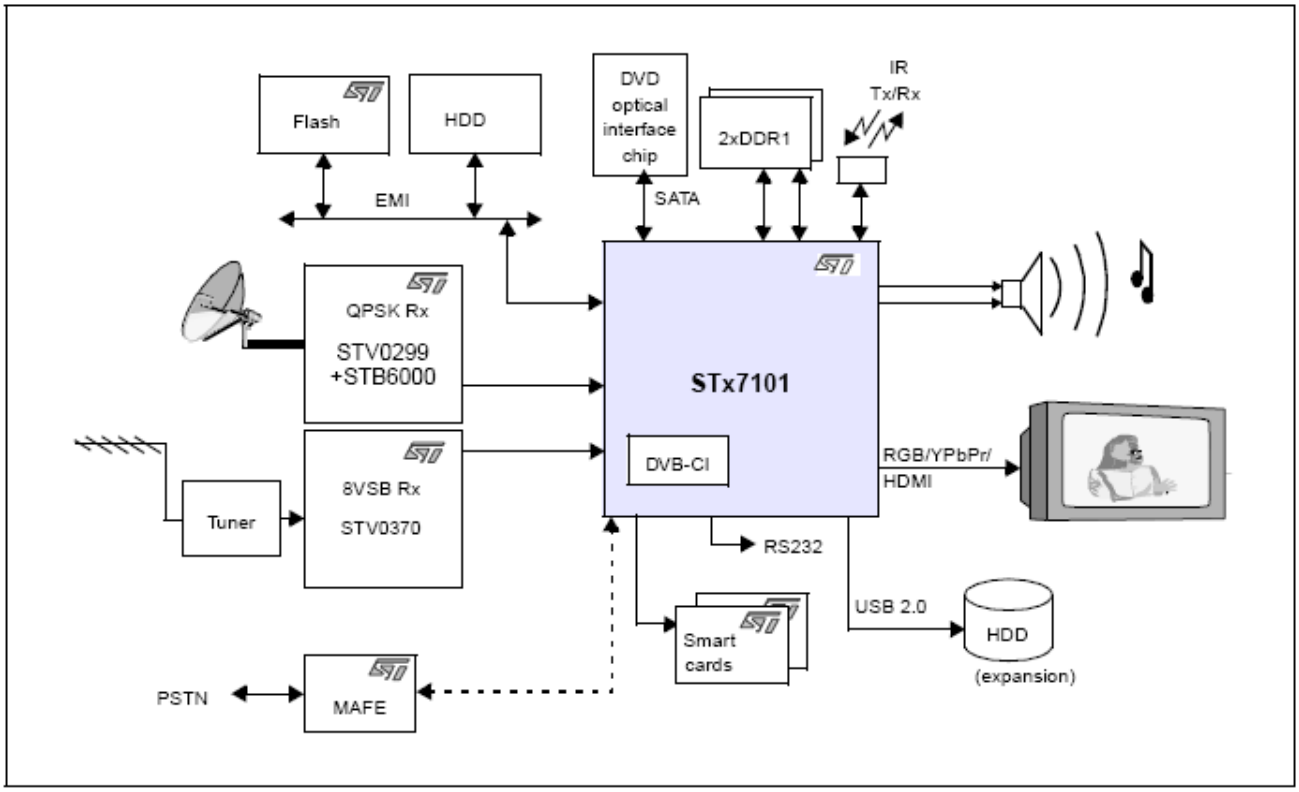
The STi7101 is a new generation, high-definition IDTV / set-top box / DVD decoder chip, and provides very high performance for low-cost HD systems. STx7101 includes an H.264 video decoder for new, low bit rate applications. Based on the Omega2 (STBus) architecture, this system-on-chip is a full back-end processor for digital terrestrial, satellite, cable, DSL and IP

client high-definition set-top boxes, compliant with ATSC, DVB, DIRECTV, DCII, OpenCable and ARIB BS4 specifications. It includes all processing for DVD applications.

The STx7101 demultiplexes, decrypts and decodes HD or SD video streams with associated multi-channel audio. Video is output to two independently formatted displays: a full resolution display intended for a TV monitor, and a downsampled display intended for a VCR or DVD-R. Connection to a TV or display panel can be analog through the DACs, or digital through a copy protected DVI/HDMI. Composite outputs are provided for connection to the VCR with Macrovision protection. Audio is output with optional PCM mixing to an S/PDIF interface, PCM interface, or through integrated stereo audio DACs. Digitized analog programs can also be input to the STx7101 for reformatting and display. The STx7101 includes a graphics rendering and display capability with a 2D graphics accelerator, three graphics planes and a cursor plane. A dual display compositor provides mixing of graphics and video with independent composition for each of the TV and VCR/DVD-R outputs. The STx7101 includes a stream merger to allow seven different transport streams from different sources to be merged and processed concurrently. Applications include DVR time-shifted viewing of a terrestrial program, while acquiring an EPG/data stream from a satellite or cable front end.

The flexible descrambling engine is compatible with required standards including DVB, DES, AES and Multi2. The STx7101 embeds a 266 MHz ST40-202 CPU for applications and device control. A dual DDR1 SDRAM memory interface is used for higher performance, to allow the video decoder the required memory bandwidth for HD H.264 and sufficient bandwidth for the CPU and the rest of the system. A second memory bus is also provided for flash memory, storing resident software, and for connection of peripherals. This bus also has a high speed synchronous mode that can be used to exchange data between two STx7101 devices. This can be used to connect a second STx7101 as a co-decoder for a dual TV STB application. A hard-disk drive (HDD) can be connected either to the serial ATA interface, or as an expansion drive through the USB 2.0 port.

The figure below shows the architecture of the Sti7101.



6.2 Features

The STx7101 is a single-chip, high definition video decoder including:

_ H.264 support
_ Linux® and OS21 compatible ST40 CPU core: 266 MHz
_ transport filtering and descrambling
_ video decoder: H.264 (MPEG-4 part 10) and MPEG-2
_ SVP compliant
_ graphics engine and dual display: standard and highdefinition
_ audio decoder
_ DVD data retrieval and decryption

The STx7101 also features the following embedded interfaces:

_ USB 2.0 host controller/PHY interface
_ DVI/HDMI™ output
_ digital audio and video auxiliary inputs
_ low-cost modem
_ 100BT ethernet controller with integrated MAC and MII/ RMII interface for external PHY
_ serial ATA (SATA)

Processor subsystem

_ ST40 32-bit superscaler RISC CPU
_ 266 MHz, 2-way set associative 16-Kbyte ICache, 32-Kbyte DCache, MMU
_ 5-stage pipeline, delayed branch support
_ floating point unit, matrix operation support
_ debug port, interrupt controller

Transport subsystem

_ TS merger/router
_ 2 serial/parallel inputs
_ 1 bidirectional interface
_ merging of 3 external transport streams
_ transport streams from memory support
_ NRSS-A module interface
_ TS routing for DVB-CI and CableCARD modules
_ Programmable transport interfaces (PTIs)
_ two programmable transport interfaces
_ two transport stream demultiplexers: DVB, DIRECTV®, ATSC, ARIB, OpenCable, DCII
_ integrated DES, AES, DVB and Multi2 descramblers
_ NDS random access scrambled stream protocol (RASP) compliant
_ NDS ICAM CA
_ support for VGS, Passage and DVS042 residue handling

Video/graphics subsystem

_ H.264(MPEG-4 part 10) main and high profile level 4.1/MPEG-2 MP@HL video decoder
_ advanced error concealment and trick mode support
_ dual MPEG-2 MP@HL decode
_ SD digital video input
_ Displays
_ one HD display multi format capable (1080I, 720P, 480P/576P, 480I/576I)
  - analog HD output RGB or YPbPr
  - HDMI encoded output
_ one standard-definition display
  - analog SD output: YPbPr or YC and CVBS
_ Gamma 2D/3D graphics processor
_ triple source 2D gamma blitter engine
_ alpha blending and logical operations
_ color space and format conversion
_ fast color fill
_ arbitrary resizing with high quality filters
_ acceleration of direct drawing by CPU
_ Gamma compositor and video processor
_ 7-channel mixer for high definition output
_ independent 2-channel mixer for SD output
_ 3 graphic display planes
_ high-quality video scaler

_ motion and detail adaptive deinterlacer
_ linear resizing and format conversions
_ horizontal and vertical filtering
_ Copy protection
_ HDMI /HDCP copy protection hardware
_ SVP compliant
_ Macrovision® copy protection for 480I, 480P, 576I, 576P outputs
_ DTCP-IP
_ AWG-based DCS analog copy protection

Audio subsystem

_ Digital audio decoder
_ support for all the most popular audio standards including MPEG-1 layer I/II, MPEG-2 layer II, MPEG-2 AAC, MPEG- 4 AAC LC 2-channel/5.1 channel MPEG-4 AAC+SBR 2-channel/5.1 channel, Dolby® Digital EX, Pro Logic® II, MLP™ and DTS®
_ PCM mixing with internal or external source and sample rate conversion
_ 6- to 2-channel downmixing
_ PCM audio input
_ independent multichannel PCM output, S/PDIF output and analog output
_ Stereo 24-bit audio DAC for analog output
_ IEC958/IEC1937 digital audio output interface (S/PDIF)
_ CSS/CPxM copy protection hardware Interfaces
_ External memory interface (EMI)
_ 16-bit interface supporting ROM, flash, SFlash, SRAM, peripherals
_ access in 5 banks
_ high speed synchronous mode for interconnecting two STx7101 devices
_ External microprocessor interface (EMPI)
_ 32-bit MPX satellite, target-only interface,
_ synchronous operation at MPX clock speed, capable of 100 MHz,
_ Dual local memory interface (LMI)
_ dual interface (2 x 32-bit) for DDR1 200-MHz (DDR400) memories,
supports 128-, 256- and 512-Mbit devices
_ USB 2.0 host controller/PHY interface
_ Serial ATA hard-disk drive support
_ record and playback with trick modes
_ pause and time shifting, watch and record
_ 100BT Ethernet controller, MAC and MII/RMII
_ On-chip peripherals
_ 4 ASCs (UARTs) with Tx and Rx FIFOS, two of which can be used in smartcard interfaces
_ 2 smartcard interfaces and clock generators (improved to reduce external circuitry)
_ 3 SSCs for I²C/SPI master slaves interfaces
_ serial communications interface (SCIF)
_ 2 PWM outputs
_ teletext serializer and DMA module
_ 6 banks of general purpose I/O, 3.3 V tolerant
_ SiLabs line-side (DAA) interface
_ modem analog front end (MAFE) interface
_ infrared transmitter/receiver supporting RC5, RC6 and RECS80 codes

_ UHF remote receiver input interface
_ interrupt level controller and external interrupts, 3.3 V tolerant
_ low power/RTC/watchdog controller
_ integrated VCXO
_ DiSEqC 2.0 interface
_ PWM capture/compare functions
_ Flexible multi-channel DMA Services and package
_ JTAG/TAP interface, ST40 toolset support, ST231 toolset support
_ Package
_ 35 x 35 PBGA, 580 + 100 balls (standard version)

6.3 Absolute Maximum Ratings

Symbol	Parameter	Min	Typical	Max	Units
Tstg	Storage temperature	- 60		150	°C
VDDE2V5	Digital 2.5 volt power supply	2.2	2.5	2.7	V
VDDE3V3	Digital 3.3 volt power supply	3.0	3.3	3.6	V
VDD	Digital core power supply	0.9	1.0	1.1	V

I/O specifications 3.3 volt pads

Symbol	Parameter	Min	Typ	Max	Units
Vil	Low level input voltage	-	-	0.8	V
Vih	High level input voltage	2	-	-	V
Vhyst	Schmitt trigger hysteresis	300	-	800	mV
Vol	Low level output voltage	-	-	0.3	V
Voh	High level output voltage	Vdde3v3 - 0.3	-	-	V
Ipu	Pull-up current (conditions Vi = 0V)	44	-	122	µA
Ipd	Pull-down current (conditions Vi = VDDE3V3	29	-	122	µA
Rpu	Equivalent pull-up resistance (conditions Vi = 0V)	29	-	67	kΩ
Rpd	Equivalent pull-down resistance (conditions Vi = VDDE3V3)	29	-	103	kΩ

I/O specifications 2.5 volt pads

Symbol	Parameter	Min	Typ	Max	Units
Vil	Low level input voltage	-	-	0.7	V
Vih	High level input voltage	1.7	-	-	V
Vhyst	Schmitt trigger hysteresis	363	-	577	mV

7 DVB-T DEMODULATOR – STV0362

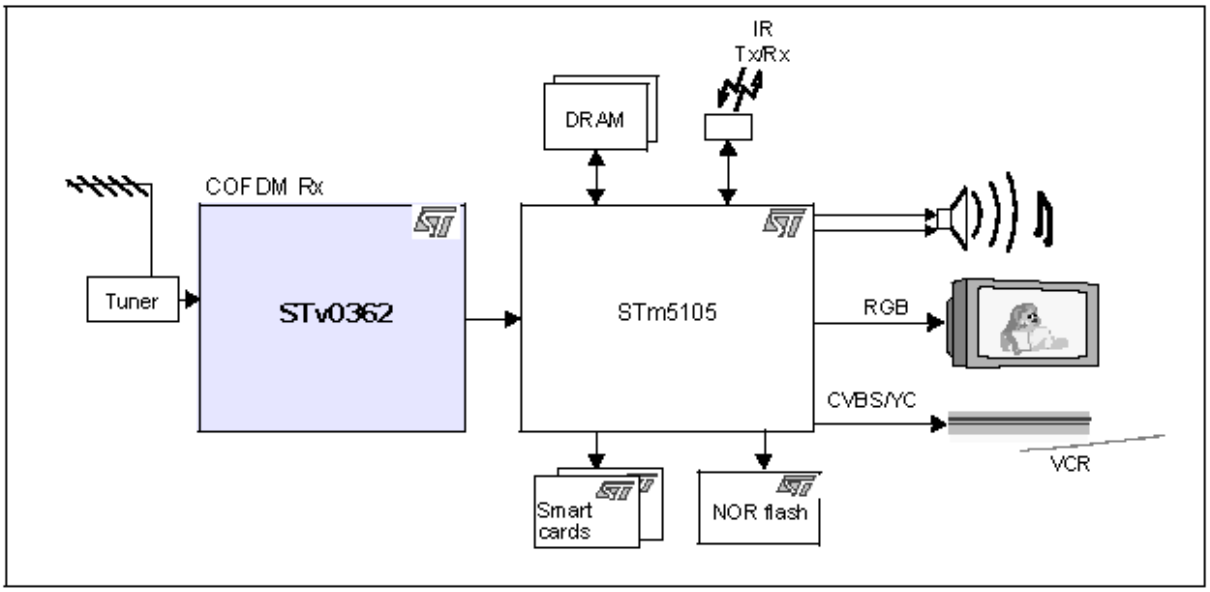
8.1 General Description

The STv0362 is a single-chip demodulator using coded orthogonal frequency division multiplexing (COFDM) and is intended for digital terrestrial receivers using compressed video, sound and data services. It converts IF or baseband differential signals to MPEG-2 format by processing OFDM carriers.

The STv0362 is fully compliant with the DVB-T specification (ETS 300 744) and NorDig Unified specification. The chip implements all the functions to convert the signals from the IF or direct conversion tuner, to produce the MPEG-2 transport stream output; in terms of IF tuner configuration, the chip is compatible with the popular STV0360/STV0361. The STv0362 offers improved performance over the STV0360 with respect to:

- channel estimation and correction,
- an extended CRL frequency and TRL timing offset,
- additional features such as:
    - synchronization for echo outside GI,
    - impulse noise rejection,
    - PLL allowing 4 MHz quartz usage.

The STv0362 processes 2, 4 and 8 K modes and integrates two A/D converters capable of handling up to 64 QAM carriers in a direct IF or zero IF sampling architecture. This eliminates the need for an external downconverter. A 12-bit ADC, intended for RF signal strength indication, eliminates the need for external components when using wide-band AGC tuners. In addition to the demodulation and forward error correction (FEC) functions required for recovery of the QAM modulated bit streams with very low BER, the chip also includes several features that give easy and immediate access to various quality monitoring parameters or lock status. The STv0362 also provides delayed AGC and a noise-free I2C bus dedicated to tuner control, which facilitate the design of high quality integrated receiver decoders. The STv0362 outputs an error-corrected MPEG-2 transport stream that complies with the DVB common interface format with programmable data clock frequency.



The STv0362 features the full DVB-T and DVB-H standards framing structure, channel coding and modulation. The symbol, timing and carrier recovery loops are fully digital and sized with regard to the state-of-the-art RF down-converting devices.

The STv0362 is compatible with direct conversion tuners featuring two differential ADC for I and Q channels. The tuner baseband power is controlled by a classic AGC loop, and the radio frequency level is monitored by a dedicated single-ended 8-bit ADC. It is recommended the RF power is left under the tuner's control, but it can be derived from baseband power by a dedicated power split algorithm. If required, the tuner serial I2C bus can be isolated by the STv0362 I2C bus repeater.

The terrestrial DVB-T network can be subjected to several interference sources which are the neighboring digital and analog channels, as well as the in-band analog channels. The STv0362 cancels these interference sources as well removing the effects of impulse noise. The channel equalization is capable of static and dynamic echo cancelling even in severe urban environments. The embedded algorithms are enhanced to cope with out-of-guard interval echoes; specific channel quality monitoring is available for acquisition and survey. The specific power handling constraints are primarily addressed by both technology and clock rate management. The efficiency of channel acquisition and re-acquisition, minimizes power consumption.

8.2 Features

- Compatible with direct conversion (ZIF) and IF tuners
  - Wide range carrier tracking loop for offset recovery
  - Dual analog to digital conversion for IQ baseband interface
  - Signal strength indicator dedicated ADC
  - Dual ΣΔ digital split AGC for RF and BB
  - Flexible clock generation to operate with 4 MHz to 27 MHz external reference

- Channel management
  - NorDig Unified Specification (v1.0.2) capable
  - Dynamic fading compatible
  - Urban environment compatible
  - Channel reception quality indicator
  - Out of guard interval echoes compatible
  - Impulsive noise rejection capable
  - Outstanding adjacent and co-channel rejection capability with integrated channel filters

- Digital carrier, timing and symbol recovery loops

- Decoding
  - 2K, 4K, 8K FFT length
  - 6, 7 and 8 MHz channels bandwidth
  - 1/4, 1/8, 1/16, 1/32 guard interval length
  - QPSK - 16 QAM - 64 QAM modulations
  - Hierarchical capability
  - TPS decoding
  - Viterbi soft decoder rate 1/2
  - Puncture rates are 1/2, 2/3, 3/4, 5/6, 7/8
  - Outer Reed-Solomon decoder as per DVB-T system
  - Energy dispersal descrambler

- Technology
  - Low power CMOS process (90nm)
  - Multi supply: 1.0 V core, 2.5 V analog, 3.3 V digital interface
  - TQFP64 7x7x1.0 mm
  - Power consumption: 350 mW (typ),
  - Standby < 80 mW

- Data to transport decoder
  - DVB common interface compliant
  - 12-bit parallel and 5-bit serial data interface with data on D7 (packet error private line)
  - Automatic regulation of the transport bit
  - rate with regard to transport clock
  - Up to 33 Mbit/s payload data rate

- I2C serial bus interface
  - Fast I2C up to 400 kHz slave interface
  - Four possible slave addresses
  - Up to 400 kbit/s private repeater for tuner isolation

- GPIOs and interruption line
  - Lock indicators: AGC, symbol, TPS, VITERBI-decoder and transport synchronization
  - ΣΔ analog and logical levels generation

- Monitoring through I2C serial interface
  - C/N estimator
  - Constellation and frequency response display
  - BER and PER estimator

8.3 Absolute Maximum Rating

Symbol	Parameter	Value	Unit
V_{dd_1v0}	DC supply voltage	-0.1, +2.2	V
V_{dd_2v5}	DC supply voltage	-0.25, +2.75	V
V_{dd_3v3}	DC supply voltage	-0.3, +3.63	V
V_{in}	Voltage on input pins	-0.3, V_{dd_3V3} +0.3	V
t_{oper}	Operating ambient temperature	-10, +70	°C
t_{stg}	Storage temperature	-40, +150	°C
t_j	Junction temperature	+125	°C

1. These are maximum limits. Exceeding them may result in permanent damage to the device. Operation at these limits is not intended.

Symbol	Parameter	Maximum value	Unit
$r_{th(j-a)}$	Junction-ambient thermal resistance	21[1]	°C/W
$r_{th(j-c)}$	Junction-case thermal resistance	TBD	°C/W

1. Four-layer PCB

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V_{dd_1v0}	Digital core supply voltage	0.9	1.0	1.1	V
V_{dd_3v3}	Digital pads supply voltage	3.0	3.3	3.6	V
V_{dda_1v0}	Analog supply voltage	0.9	1.0	1.1	V
V_{dda_2v5}	Analog supply voltage	2.25	2.5	2.75	V
I/Os					
V_{il} V_{ih}	Input logic low Input logic high	-0.5 2.0		0.8 3.6	V V
V_{ol} V_{oh}	Output logic low Output logic high	-0.5 2.4		0.3 3.6	V V
i_{lk}	Input leakage current (V_{in} = 0 V to 3.3 V)	TBD	TBD	TBD	µA
i_{ol}	Output sink current	TBD	TBD	TBD	µA

Symbol	Parameter	Min	Typ	Max	Unit
f_{clk_in}	CLKI or XTAL frequency	4	27	28	MHz
Idd_1V0	Current consumption (1.0 V)		TBD		mA
Idd_3V3	Current consumption (3.3 V)		TBD		mA
Idd_2V5	Current consumption (2.5 V)		TBD		mA
P_{max}	Maximum power			350	mW

8.4 Pinning

Pin number	Name	Pin number	Name
1	RF_LEVEL	33	D0
2	VDDA_2V5	34	VDD_3V3
3	QP	35	D1
4	QM	36	D2
5	VDDA_ISO	37	D3
6	VDDA_2V5	38	VDD_1V0
7	REFP	39	D4
8	REFM	40	D5
9	INCM	41	VDD_3V3
10	IM	42	D6
11	IP	43	D7
12	VDDA_1V0	44	CLK_OUT
13	VDDA_2V5	45	VDD_1V0
14	XTAL_O	46	STR_OUT
15	XTAL_I	47	D/NOT_P
16	VDDA_2V5	48	ERROR
17	AGC_IF	49	GPIO1
18	AGC_RF	50	VDD_3V3
19	VDD_1V0	51	VDD_1V0
20	SCLT	52	GPIO8
21	SDAT	53	GPIO7
22	VDD_3V3	54	GPIO6
23	AUX_CLK	55	VDD_1V0
24	VDD_1V0	56	VDD_3V3
25	CS0	57	GPIO5
26	CS1	58	GPIO4
27	GPIO0	59	GPIO3
28	VDD_3V3	60	GPIO2
29	SDA	61	GPIO9
30	SCL	62	VDD_1V0
31	VDD_1V0	63	VDD_3V3
32	NOT_RESET	64	TEST

8 DVB-C DEMODULATOR – STV0297E

8.1 General Desription

The STV0297E is a complete single-chip QAM (quadrature amplitude modulation) demodulation and FEC (forward error correction) solution that performs sampled IF to transport stream (MPEG-2 or MPEG-4) block processing of QAM signals. It is intended for the digital transmission of compressed television, sound, and data services over cable. It is fully compliant with ITU-T J83 Annexes A/C or DVB-C specification bitstreams (ETS 300 429, “Digital broadcasting systems for television, sound and data services – Framing structure, channel coding and modulation - Cable Systems”). It can handle square (16, 64, 256-QAM) and non-square (32, 128-QAM) constellations. Japanese DBS systems require a transport stream multiplex frame (TSMF) layer to carry digital signals over cable systems. When the recovered transport stream is a multiplex frame, the STV0297E post-processes it to extract a single transport stream. Automatic detection of the TSMF layer is provided. The chip integrates an analog-to-digital converter that delivers the required performance to handle up to 256-QAM signals in a direct IF sampling architecture, thus eliminating the need for external downconversion.

8.2 Features

- Decodes ITU-T J.83-Annexes A/C and DVB-C bit streams
- Processes Japanese transport stream multiplex frame (TSMF)
- High-performance integrated A/D converter suitable for direct IF architecture in all QAM (quadrature amplitude modulation) modes
- Supports 16, 32, 64, 128 and 256 point constellations
- Small footprint package: (10 x 10 mm²)
- Very low power consumption
- Full digital demodulation
- Variable symbol rates
- Front derotator for better low symbol rate performance and relaxed tuner constraints
- Integrated matched filtering
- Robust integrated adaptive pre and post equalizer
- On-chip FEC A/C with ability to bypass individual blocks
- 10 programmable GPIO
- Two AGC outputs suitable for delayed AGC applications (sigma-delta outputs)
- Integrated signal quality monitors, plus lock indicator and interrupt function mapped to GPIO pin
- Improved signal acquisition
- System clock generated on-chip from quartz crystal
- Low frequency crystal operations 4, 16, 25 - 30 MHz
- 4 I2C addresses
- Easy control and monitoring via 2-wire fast I2C bus

8.3 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD_1V0}	DC supply voltage	-0.1, +1.1	V
V_{DD_2V5}	DC supply voltage	-0.25, +2.75	V
V_{DD_3V35}	DC supply voltage	-0.5, +3.63	
V_{IN_D}	Voltage on digital input pins	-0.3, $V_{DD_}$3V3 + 0.3	V
V_{IN_A}	Voltage on analog input pins	0.3, $V_{DD_}$2V5 + 0.3	V
T_{OPER}	Operating ambient temperature	0, +70	°C
T_{STG}	Storage temperature	-40, +150	°C
Tj	Junction temperature	+125	°C

8.4 Pinning

Pad num	Name	Type	Drive
1	GPIO9	digital	2mA
2	GPIO8	digital	2mA
3	TDI	digital	2mA
4	TDO	digital	2mA
5	TRST	digital	2mA
6	TCK	digital	2mA
7	TMS	digital	2mA
8	GPIO7/AUX_CLK	digital	2mA
9	N_RESET	digital	2mA
10	VDD	dig. supply	
11	GND	dig. supply	
12	VDD_IO_3V3	dig. supply 3.3v	
13	GPIO6/CS0	digital	2mA
14	GPIO5/CS1	digital	2mA
15	SDA	digital	2mA
16	SCL	digital	2mA
17	M_CKOUT	digital	4mA
18	M_SYNC	digital	2mA
19	M_VALID	digital	4mA
20	M_ERR	digital	2mA
21	TS_DATA[0]	digital	4mA
22	TS_DATA[1]	digital	2mA
23	TS_DATA[2]	digital	2mA
24	TS_DATA[3]	digital	2mA
25	VDD	dig. supply	
26	GND	dig. supply	
27	VDD_IO_3V3	dig. supply 3.3v	
28	TS_DATA[4]	digital	2mA
29	TS_DATA[5]	digital	2mA
30	TS_DATA[6]	digital	2mA
31	TS_DATA[7]	digital	4mA
32	GPIO4/SDAT	digital	2mA

Pad num	Name	Type	Drive
33	GPIO3/SCLT	digital	2mA
34	GPIO2	digital	2mA
35	GPIO1/AGC1	digital	2mA
36	GPIO0/AGC2	digital	2mA
37	VDD	dig. supply	
38	GND	dig. supply	
39	VDD_IO_3V3	dig. supply 3.3v	
40	GNDAS_AD	analog gnd	
41	INM	analog	
42	INP	analog	
43	VCCAISO_D	anal. 2.5v supply	
44	INCM	analog	
45	REFM	analog	
46	REFP	analog	
47	GNDA_AD12	analog ground	
48	VCCA_AD12	analog supply	
49	GNDD_AD12	analog ground	
50	VCCD_AD12	anal. 1.0v supply	
51	GNDA_PLL	analog ground	
52	VCCA_PLL	anal. 2.5v supply	
53	GNDD_PLL	analog ground	
54	VCCD_PLL	anal.1.0v supply	
55	ZO		
56	VCCA_OSC	anal. 2.5v supply	
57	A		
58	GNDA_OSC	analog ground	
59	VBASE		
60	VDD10REG		
61	VDD	dig. supply	
62	GND	dig. supply	
63	VDD_IO_3V3	dig. supply 3.3v	
64	CLK_TST	digital	4mA

9 HY5DV281622DT-5 DDR SDRAM 128M

9.1 General Description

The Hynix HY5DV281622 is a 134,217,728-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the point-to-point applications which requires high bandwidth. The Hynix 8Mx16 DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data,Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2.

9.2 Features

- 3.3V for VDD and 2.5V for VDDQ power supply
- All inputs and outputs are compatible with SSTL_2 interface
- JEDEC standard 400mil 66pin TSOP-II with 0.65mm pin pitch
- Fully differential clock inputs (CK, /CK) operation
- Double data rate interface
- Source synchronous - data transaction aligned to bidirectional data strobe (DQS)
- x16 device has 2 bytewide data strobes (LDQS, UDQS) per each x8 I/O
- Data outputs on DQS edges when read (edged DQ) Data inputs on DQS centers when write (centered DQ)
- Data(DQ) and Write masks(DM) latched on the both rising and falling edges of the data strobe
- All addresses and control inputs except Data, Data strobes and Data masks latched on the rising edges of the clock
- Write mask byte controls by LDM and UDM
- Programmable /CAS latency 3 / 4 supported
- Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
- Internal 4 bank operations with single pulsed /RAS
- tRAS Lock-Out function supported
- Auto refresh and self refresh supported
- 4096 refresh cycles / 32ms
- Full, Half and Matched Impedance(Weak) strength driver option controlled by EMRS

9.3 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-0.5 ~ 3.6	V
Voltage on VDD relative to VSS	VDD	-0.5 ~ 3.6	V
Voltage on VDDQ relative to VSS	VDDQ	-0.5 ~ 3.6	V
Output Short Circuit Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · sec

9.4 Pinning

PIN	TYPE	DESCRIPTION
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, excluding CK, /CK and CKE are disabled during POWER DOWN. Input buffers, excluding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied.
/CS	Input	Chip Select : Enables or disables all inputs except CK, /CK, CKE, DQS and DM. All commands are masked when CS is registered high. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.
A0 ~ A11	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
/RAS, /CAS, /WE	Input	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
LDM, UDM	Input	Input Data Mask: DM(LDM,UDM) is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. LDM corresponds to the data on DQ0-Q7; UDM corresponds to the data on DQ8-Q15.
LDQS, UDQS	I/O	Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. LDQS corresponds to the data on DQ0-Q7; UDQS corresponds to the data on DQ8-Q15.
DQ0 ~ DQ15	I/O	Data input / output pin : Data Bus
VDD/VSS	Supply	Power supply for internal circuits and input buffers.
VDDQ/VSSQ	Supply	Power supply for output buffers for noise immunity.
VREF	Supply	Reference voltage for inputs for SSTL interface.
NC	NC	No connection.

10 HY5DU561622ETP-5 DDR SDRAM 256M

11.1 General Description

The Hynix HY5DU561622DTP is a 268,435,456-bit CMOS Double Data Rate(DDR) Synchronous DRAM, ideally suited for the point-to-point applications which requires high bandwidth. The Hynix 16Mx16 DDR SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the /CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 2-bit prefetched to achieve very high bandwidth. All input and output voltage levels are compatible with SSTL_2.

11.2 Features

• 2.5V +/-5% VDD and VDDQ power supply
supports 200 / 166MHz
• All inputs and outputs are compatible with SSTL_2 interface
• JEDEC standard 400mil 66pin TSOP-II with 0.65mm pin pitch
• Fully differential clock inputs (CK, /CK) operation
• Double data rate interface
• Source synchronous - data transaction aligned to bidirectional data strobe (DQS)
• x16 device has 2 bytewide data strobes (LDQS,UDQS) per each x8 I/O
• Data outputs on DQS edges when read (edged DQ)
Data inputs on DQS centers when write (centered DQ)
• Data(DQ) and Write masks(DM) latched on the both rising and falling edges of the data strobe
• All addresses and control inputs except Data, Data strobes and Data masks latched on the rising edges
of the clock
• Write mask byte controls by LDM and UDM
• Programmable /CAS latency 3 / 4 supported
• Programmable Burst Length 2 / 4 / 8 with both sequential and interleave mode
• Internal 4 bank operations with single pulsed /RAS
• tRAS Lock-Out function supported
• Auto refresh and self refresh supported
• 8192 refresh cycles / 64ms
• Full, Half and Matched Impedance(Weak) strength driver option controlled by EMRS

11.3 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Ambient Temperature	T_A	0 ~ 70	°C
Storage Temperature	T_{STG}	-55 ~ 125	°C
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.5 ~ 3.6	V
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.5 ~ 3.6	V
Output Short Circuit Current	I_{OS}	50	mA
Power Dissipation	P_D	1	W
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · sec

Note : Operation at above absolute maximum rating can adversely affect device reliability

11.4 Pinning

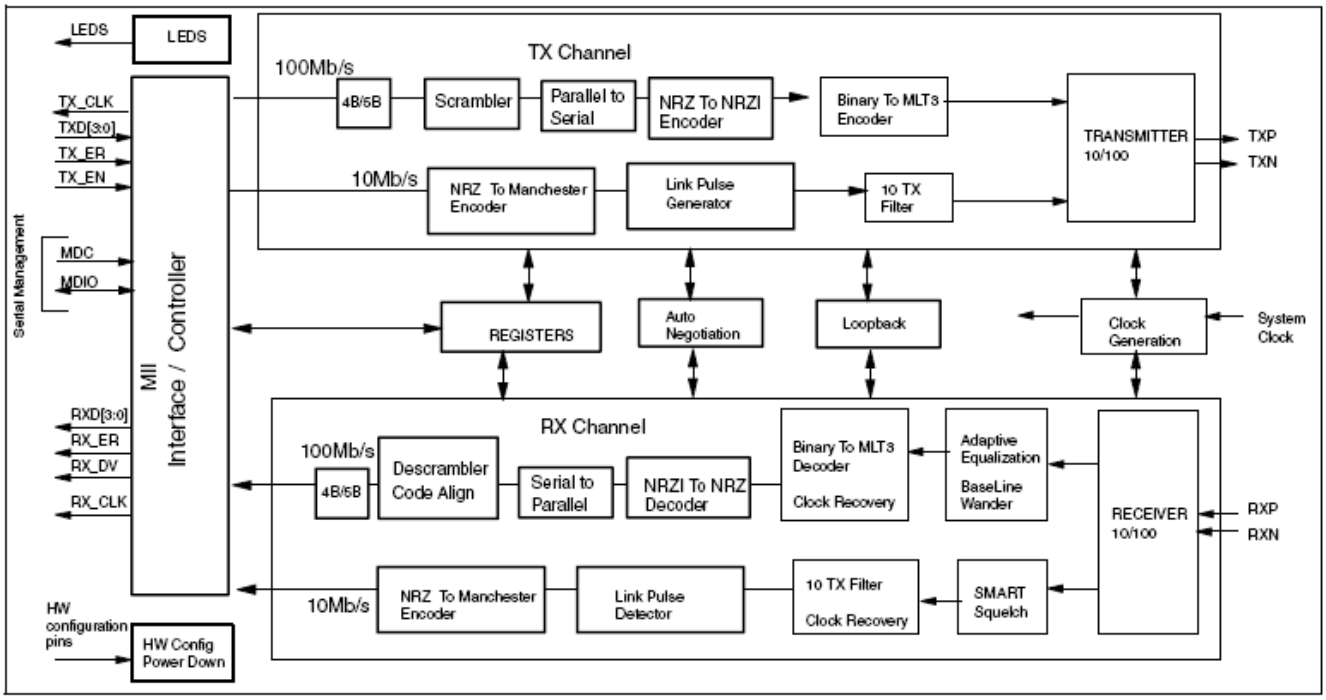
PIN	TYPE	DESCRIPTION
CK, /CK	Input	Clock: CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output (read) data is referenced to the crossings of CK and /CK (both directions of crossing).
CKE	Input	Clock Enable: CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for POWER DOWN entry and exit, and for SELF REFRESH entry. CKE is asynchronous for SELF REFRESH exit, and for output disable. CKE must be maintained high throughout READ and WRITE accesses. Input buffers, exduding CK, /CK and CKE are disabled during POWER DOWN. Input buffers, exduding CKE are disabled during SELF REFRESH. CKE is an SSTL_2 input, but will detect an LVCMOS LOW level after Vdd is applied.
/CS	Input	Chip Select : Enables or disables all inputs except CK, /CK, CKE, DQS and DM. All commands are masked when CS is registered high. CS provides for external bank selection on systems with multiple banks. CS is considered part of the command code.
BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.
A0 ~ A12	Input	Address Inputs: Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 is sampled during a precharge command to determine whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op code during a MODE REGISTER SET command. BA0 and BA1 define which mode register is loaded during the MODE REGISTER SET command (MRS or EMRS).
/RAS, /CAS, /WE	Input	Command Inputs: /RAS, /CAS and /WE (along with /CS) define the command being entered.
LDM, UDM	Input	Input Data Mask: DM(LDM,UDM) is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. LDM corresponds to the data on DQ0-Q7; UDM corresponds to the data on DQ8-Q15.
LDQS, UDQS	I/O	Data Strobe: Output with read data, input with write data. Edge aligned with read data, centered in write data. Used to capture write data. LDQS corresponds to the data on DQ0-Q7; UDQS corresponds to the data on DQ8-Q15.
DQ0 ~ DQ15	I/O	Data input / output pin : Data Bus
VDD/VSS	Supply	Power supply for internal circuits and input buffers.
VDDQ/VSSQ	Supply	Power supply for output buffers for noise immunity.
VREF	Supply	Reference voltage for inputs for SSTL interface.
NC	NC	No connection.

11 STE100P Ethernet PHY

11.1 General Description

The STE100P, also referred to as STEPHY1, is a high performance Fast Ethernet physical layer interface for 10Base-T and 100Base-TX applications. It was designed with advanced CMOS technology to provide a Media Independent Interface (MII) for easy attachment to 10/100 Media Access Controllers (MAC) and a physical media interface for 100Base-TX of IEEE802.3u and 10Base-T of IEEE802.3.

The STEPHY1 supports both half-duplex and fullduplex operation, at 10 and 100 Mbps operation. Its operating mode can be set using auto-negotiation, parallel detection or manual control. It also allows for the support of auto-negotiation functions for speed and duplex detection.



11.2 Features

- IEEE802.3u 100Base-TX and IEEE802.3 10Base-T compliant
- Support for IEEE802.3x flow control
- IEEE802.3u Auto-Negotiation support for 10Base-T and 100Base-TX
- MII interface
- Standard CSMA/CD or full duplex operation supported
- Integrates the whole Physical layer functions of 100Base-TX and 10Base-T

- Provides Full-duplex operation on both 100Mbps and 10Mbps modes
- Provides Auto-negotiation(NWAY) function of full/half duplex operation for both 10 and 100 Mbps
- Provides MLT-3 transceiver with DC restoration for Base-line wander compensation
- Provides transmit wave-shaper, receive filters, and adaptive equalizer
- Provides loop-back modes for diagnostic
- Builds in Stream Cipher Scrambler/ De-scrambler and 4B/5B encoder/decoder
- Supports external transmit transformer with turn ratio 1:1
- Supports external receive transformer with turn ratio 1:1
- Standard 64-pin QFP package pinout

11.3 Absolute Maximum Ratings

Parameter	Value
Supply Voltage(Vcc)	-0.5 V to 7.0 V
Input Voltage	-0.5 V to VCC + 0.5 V
Output Voltage	-0.5 V to VCC + 0.5 V
Storage Temperature	-65 °C to 150 °C(-85°F to 302°F)
Ambient Temperature	(-40)°C to +85°C)
ESD Protection	2000V

12.4 Pinning

Pin No.	Name	Type	Description
MII Data Interface			
52 58 57 56 55	txd4 txd3 txd2 txd1 txd0	I	**Transmit Data**. The Media Access Controller (MAC) drives data to the STE100P using these inputs. txd4 is monitored only in Symbol (5B) Mode. These signals must be synchronized to the tx_clk.
54	tx_en	I	**Transmit Enable**. The MAC asserts this signal when it drives valid data on the txd inputs. This signal must be synchronized to the tx_clk.
53	tx_clk	I/O	**Transmit Clock**. Normally the STE100P drives tx_clk. Refer to the Clock Requirements discussion in the Functional Description section. 25 MHz for 100 Mbps operation. 2.5 MHz for 10 Mbps operation.

Pin No.	Name	Type	Description
52	tx_er	I	**Transmit Coding Error**. The MAC asserts this input when an error has occurred in the transmit data stream. When the STE100P is operating at 100 Mbps, the STE100P responds by sending invalid code symbols on the line. In Symbol (5B) Mode this pin functions as txd4.
51 43 44 46 47	rxd4 rxd3 rxd2 rxd1 rxd0	O	**Receive Data**. The STE100P drives received data on these outputs, synchronous to rx_clk. rxd4 is driven only in Symbol (5B) Mode.
48	rx_dv	O	**Receive Data Valid**. The STE100P asserts This signal when it drives valid data on rxd. This output is synchronous to rx_clk.
51	rx_er	O	**Receive Error**. The STE100P asserts this output when it receives invalid symbols from the network. This signal is synchronous to rx_clk. In Symbol (5B) Mode this pin functions as rxd4.
49	rx_clk	O	**Receive Clock**. This continuous clock provides reference for rxd, rx_dv, and rx_er signals. Refer to the Clock Requirements discussion in the Functional Description section. 25 MHz for 100 Mbps operation. 2.5 MHz for 10 Mbps operation.
59	col	O	**Collision Detected**. The STE100P asserts this output when detecting a collision. This output remains High for the duration of the collision. This signal is asynchronous and inactive during full-duplex operation.
60	crs	O	**Carrier Sense**. During half-duplex operation (PR0:8=0), the STE100P asserts this output when either transmit or receive medium is non idle. During full duplex operation (PR0:8=1), crs is asserted only when the receive medium is non-idle.
MII Control Interface			
42	mdc	I	**Management Data Clock**. Clock for the mdio serial data channel. Maximum frequency is 2.5 MHz.
41	mdio	I/O	**Management Data Input/Output**, Bi-directional serial data channel for PHY communication.
61	mdint	OD	**Management Data Interrupt**. When any bit in PR18 = 1, an active High output on this pin indicates status change in the corresponding bits in PR17. Interrupt is cleared by reading Register PR17. Requires MDC edge to output.
Physical (Twisted Pair) Interface			
12	x1	I	25 MHz reference clock input. When an external 25 MHz crystal is used, this pin will be connected to one terminal of it. If an external 25 MHz clock source of oscillator is used, then this pin will be the input pin of it.
11	x2	O	25 MHz reference clock output. When an external 25MHz crystal is used, this pin will be connected to another terminal of if. If an external clock source is used, then this pin should be left open.
21 23	txp txn	O	The differential Transmit outputs of 100Base-TX or 10Base-T, these pins directly output to the transformer.
19 18	rxp rxn	I	The differential Receive inputs of 100Base-TX or 10Base-T, these pins directly input from the transformer.

Pin No.	Name	Type	Description
15	iref	O	Reference Resistor connecting pin for reference current, directly connect a 5KΩ ± 1% resistor to Vss.
38	ledr10	I/O	LED display for 10Ms/s link status. This pin will be driven on continually when 10Mb/s network operating speed is detected. The pull-up/pull-down status of this pin is latched into the PR20 bit 7 during power up/reset.
37	ledtr		LED display for Tx/Rx Activity status. This pin will be driven on at a 10 Hz blinking frequency when either effective receiving or transmitting is detected. The status of this pin is latched into the PR20 bit 6 during power up/reset.
36	ledl	I/O	LED display for Link Status. Blinks when there is TX or RX activity. This pin will be driven on continually when a good Link test is detected. The status of this pin is latched into the PR20 bit 5 during power up/reset.
35	ledc	I/O	LED display for Full Duplex or Collision status. This pin will be driven on continually when a full duplex configuration is detected. This pin will be driven on at a 20 Hz blinking frequency when a collision status is detected in the half duplex configuration. The status of this pin is latched into the PR20 bit 4 during power up/reset.
34	leds	I/O	LED display for 100Ms/s link status. This pin will be driven on continually when 100Mb/s network operating speed is detected. The status of this pin is latched into the PR20 bit 3 during power up/reset.
64	cfg0	I	Configuration Control 0. **When A/N is enabled**, cfg0 determines operating mode advertisement capabilities in combination with cfg1 when mf0/ PR0:12 =1. (See Table 2) **When A/N is disabled**, cfg1 disables mlt3 and directly affects PR19:0 When cfg0 is Low, mlt3 encoder/decoder is enabled and PR19:1 =0. When cfg0 is High, mlt3 encoder/decoder is bypassed and PR19:1 = 1.
63	cfg1	I	Configuration Control 1. **When A/N is enabled**, cfg1 determines operating mode advertisement capabilities in combination with cfg1 when mf0/ PR0:12 =1. (See Table 2) **When A/N is disabled**, CFG1 enables Loopback mode and directly affects PR0 bit 14. When cfg1 is Low, Loopback mode is disabled and PR0:14 = 0. When cfg1 is High, Loopback mode is enabled and PR0:14 = 1.
28	reset	I	**Reset** (Active-Low). This input must be held low for a minimum of 1 ms to reset the STE100P. During Power-up, the STE100P will be reset regardless of the state of this pin, and this reset will not be complete until after >1ms.
29	rip	O	**Reset In Progress**. This output is used to indicate when the device has completed power-up/reset and the registers and functions can be accessed. When rip is High, power-up/reset has been successful and the device can be used normally When rip is Low, device reset is not complete.
8, 30,31, 32	nc		nc (No Connection)
26, 33	test, test_se		Test pins. Should be tied to ground for normal operation
27	pwrdwn	I	**Power Down**. When High, forces STE100P into Power Down mode. This pin is OR'ed with the Power Down bit (PR0:11). During the Power Down mode, txp/txn outputs and all LED outputs are 3-stated, and the MII interface is isolated.

<table>
<tr><th>Pin No.</th><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>5
4
3
2
1</td><td>mf0
mf1
mf2
mf3
mf4</td><td>I</td><td>Multi-Function pins. Each mf pin internally drives different configuration functions. The functions of the five mf inputs are as shown in the table below.

<table><tr><th>Pin</th><th>Function</th><th>Register & Bit Affected</th></tr><tr><td>mf0</td><td>Auto-Negotiation</td><td>PR0:12 ANE</td></tr><tr><td>mf1</td><td>Enable NRZ-NRZI conversion</td><td>PR16:7 ENNRZI</td></tr><tr><td>mf2</td><td>4B/5B Coding Enable</td><td>PR16:6 EN4B5B</td></tr><tr><td>mf3</td><td>Scrambler Operation Disable</td><td>PR16:5 DISCRM</td></tr><tr><td>mf4</td><td>MII 10/100 Mbps Speed Select</td><td>PR0:13 SPSEL</td></tr></table>
The logic level of mf0-4 will determine the value that the affected bits will have upon reset of the STE100P. The operating functions of cfg0, cfg1, and fde change depending on the state of mf0 (Auto-Negotiation enabled or disabled). Table 2 shows the relationship between cfg0, cfg1 and fde.</td></tr>
<tr><td>6</td><td>fde</td><td>I</td><td>Full-Duplex Enable.
When A/N is enabled, fde determines full-duplex advertisement capability in combination with cfg0 and cfg1. (See Table 2)
When A/N is disabled, fde directly affects full-duplex operation and determines the value of PR0 bit 8 (Full/Half Duplex Mode Select).
When fde is High, full-duplex is enabled and PR0:8 = 1.
When fde is Low, full-duplex is disabled and PR0:8 = 0.</td></tr>
<tr><td colspan="4">Digital Power Pins</td></tr>
<tr><td>39, 45, 62</td><td></td><td colspan="2">vcce, vcce/i</td></tr>
<tr><td>25, 40, 50</td><td></td><td colspan="2">gnde, gnde/i</td></tr>
<tr><td colspan="4">Analog Power Pins</td></tr>
<tr><td>9, 13, 16, 17, 22</td><td></td><td colspan="2">vcca</td></tr>
<tr><td>7, 10, 14, 20, 24</td><td></td><td colspan="2">gnda</td></tr>
</table>

12SAW FILTER

12.1 IF Filter for Audio Applications – Epcos K9656M

12.1.1 Standart:

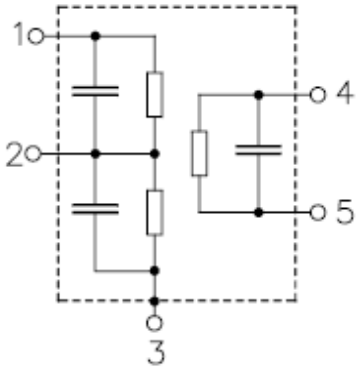
- B/G
- D/K
- I
- L/L’

12.1.2 Features:

- TV IF audio filter with two channels
- Channel 1 (L’) with one pass band for sound carriers at 40,40 MHz (L’) and 39,75 MHz (L’- NICAM)

- Channel 2 (B/G,D/K,L,I) with one pass band for sound carriers between 32,35 MHz and 33,40 MHz

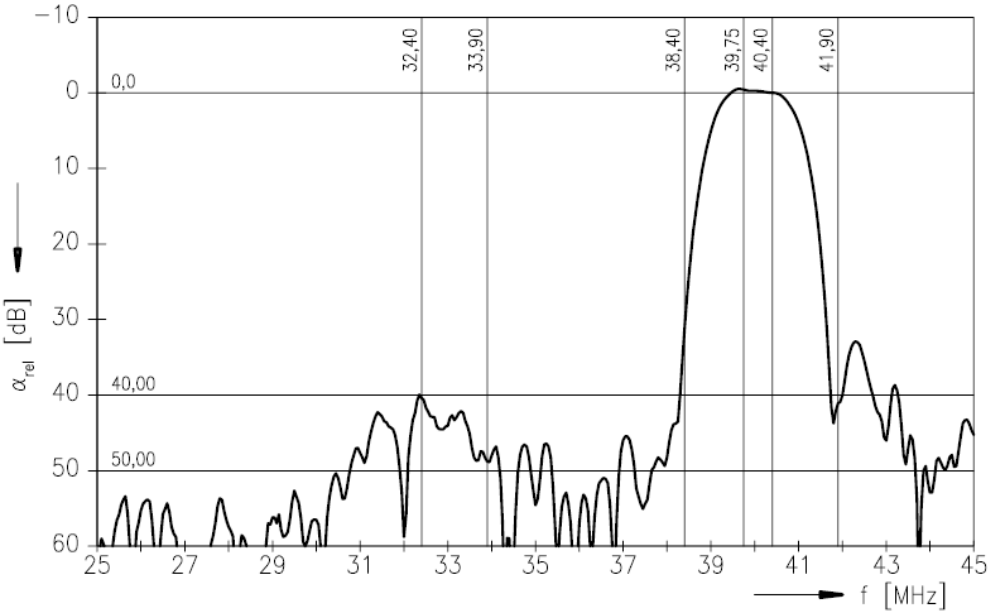
12.1.3 Pin configuration:



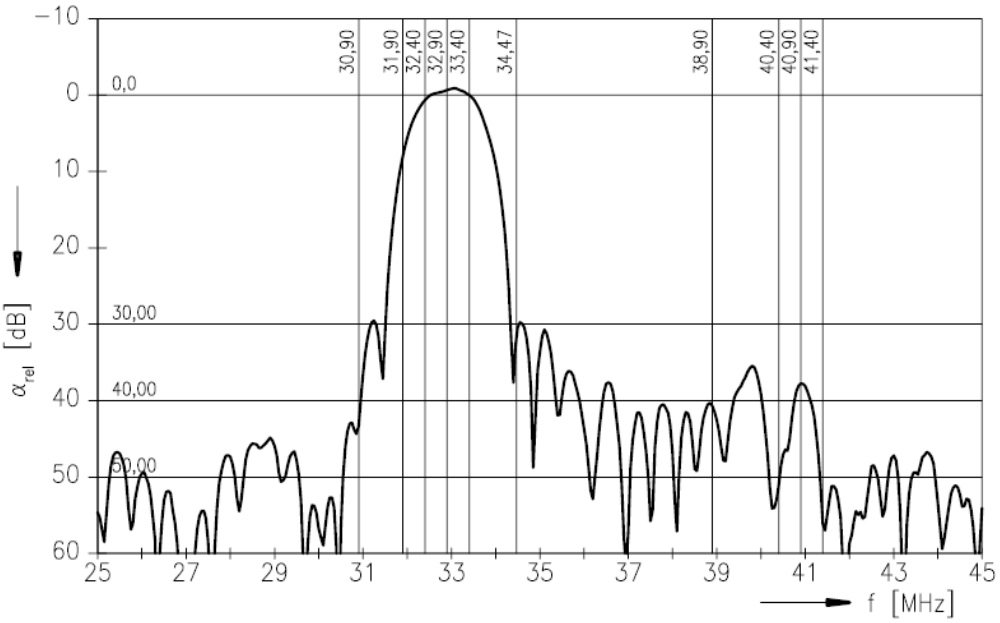
1 Input
2 Switching input
3 Chip carrier - ground
4 Output
5 Output

12.1.4 Frequency response:

Frequency response of channel 1



Frequency response of channel 2



12.2 IF Filter for Video Applications – Epcos K3958M

12.2.1 Standart:

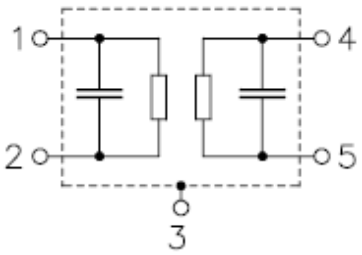
- B/G
- D/K
- I
- L/L'

12.2.2 Features:

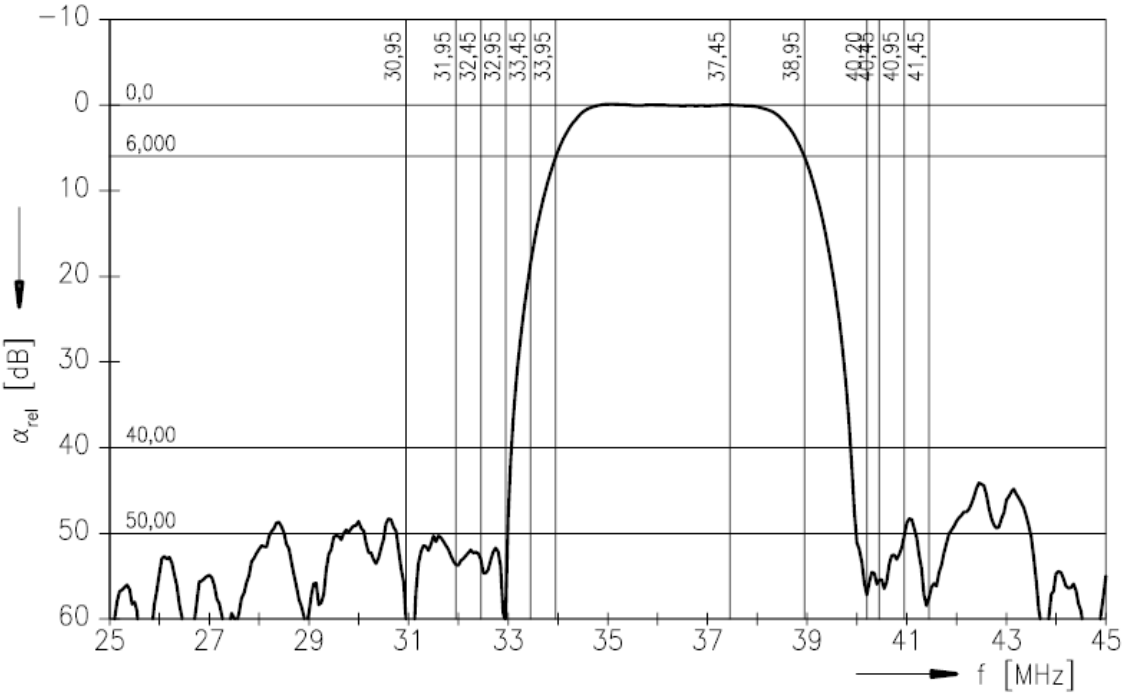
- TV IF filter with Nyquist slopes at 33.90 MHz and 38.90 MHz
- Constant group delay

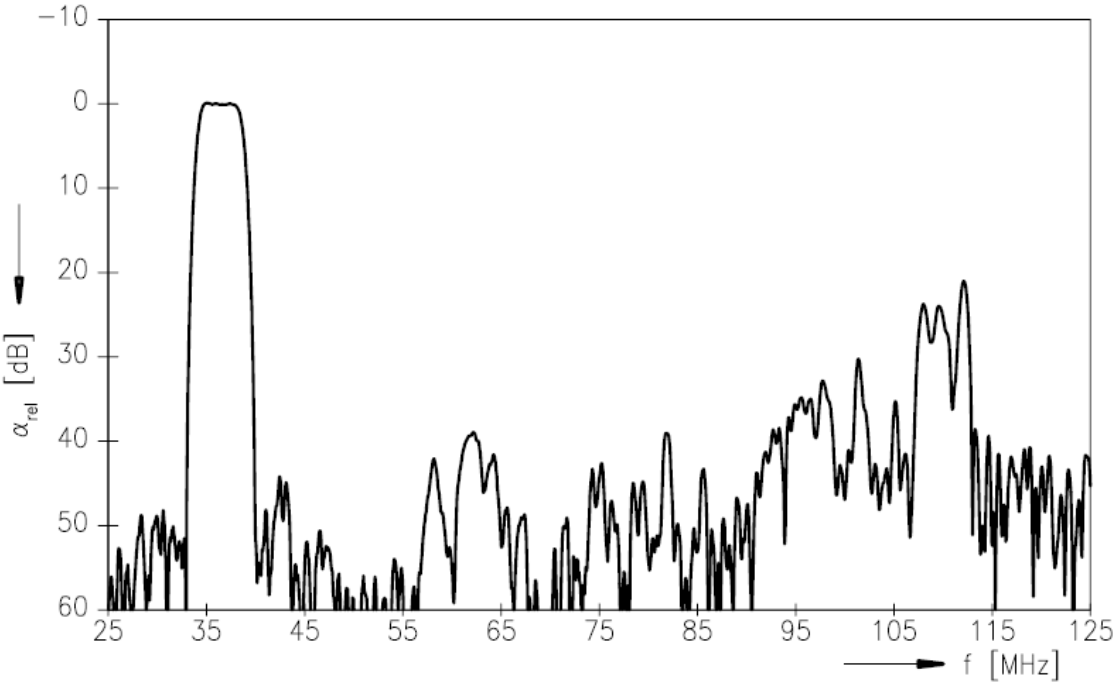
Pin configuration:

1 Input
2 Input - ground
3 Chip - carrier ground
4 Output
5 Output



12.2.3 Frequency response:





132048-Bits Serial EEPROM – 24LC02

13.1 General Description

The 24LC01/02 is a 1K/2K-bit serial read/write non-volatile memory device using the CMOS floating gate process. Its 1024/2048 bits of memory are organized into 128/256 words and each word is 8 bits. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. Up to eight HT24LC01/02 devices may be connected to the same two-wire bus. The HT24LC01/02 is guaranteed for 1M erase/write cycles and 40-year data retention.

13.2 Features

- Operating voltage: 2.4V~5.5V
- Low power consumption
- Operation: 5mA max.
- Standby: 5mA max.
- Internal organization
- 1K (HT24LC01):128´8
- 2K (HT24LC02): 256´8
- 2-wire serial interface
- Write cycle time: 5ms max.
- Automatic erase-before-write operation
- Partial page write allowed
- 8-byte Page write modes
- Write operation with built-in timer
- Hardware controlled write protection
- 40-year data retention
- 106 erase/write cycles per word
- 8-pin DIP/SOP package
- 8-pin TSSOP (HT24LC02 only)
- Commerical temperature range (0°C to +70°C)

13.3 Electrical Specifications

DC Electrical Characteristics (Vcc =2.7~5.5V, Ta = 25ºC)

Symbol	Parameter	Conditions	24LC02		Units
			Min	Max	
I_{CC1}	Operating Current (Program)	SCL = 100KHz CMOS Input Levels	—	3	mA
I_{CC2}	Operating Current (Read)	SCL = 100KHz CMOS Input Levels	—	200	µA
I_{SB1}	Standby Current	SCL=SDA=0V, Vcc=5V	—	10	µA
I_{SB2}	Standby Current	SCL=SDA=0V, Vcc=3V	—	1	
I_{IL}	Input Leakage	VIN = 0 V to VCC	-1	+1	µA
I_{OL}	Output Leakage	VOUT = 0 V to Vcc	-1	+1	µA
V_{IL}	Input Low Voltage**		-0.1	Vcc x 0.3	V
V_{IH}	Input High Voltage**		Vcc x 0.7	V_{CC}+ 0.2	V
V_{OL1}	Output Low Voltage	IOL = 2.1mA TTL	—	0.4	V
V_{OL2}	Output Low Voltage	IOL = 10uA CMOS	—	0.2	V
V_{LK}	VCC Lockout Voltage	Programming Command Can Be Executed	Default	—	V

AC Electrical Characteristics (Vcc =2.7~5.5V)

Parameter	Symbol	24LC02		Units
		Min	Max	
Clock frequency	Fscl	0	100	kHz
Clock high time	Thigh	4000	—	ns
Clock low time	Tlow	4700	—	ns
SDA and SCL rise time**	Tr	—	1000	ns
SDA and SCL fall time**	Tf	—	300	ns
START condition hold time	Thd:Sta	4000	—	ns
START condition setup time	Tsu:Sta	4700	—	ns
Data input hold time	Thd:Dat	0	—	ns
Data input setup time	Tsu:Dat	250	—	ns
STOP condition setup time	Tsu:Sto	4000	—	ns
Output valid from clock	Taa	300	3500	ns
Bus free time **	Tbuf	4700	—	ns
Data out hold time	Tdh	300	—	ns
Write cycle time	Twr	—	10	ms
5V, 25ºC, Byte Mode	Endurance**	1M	—	write cycles

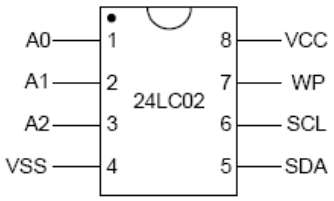
Capacitance TA= 25ºC , f=250KHz

Symbol	Parameter	Max	Units
C_{OUT}	Output capacitance	5	pF
C_{IN}	Input capacitance	5	pF

A.C. Conditions of Test

Input Pulse Levels	Vcc x 0.1 to Vcc x 0.9
Input Rise and Fall times	10 ns
Input and Output Timming level	Vcc x 0.5
Output Load	1 TTL Gate and CL = 100pf

13.4 Pinning



PDIP/SOP/TSSOP

A0, A1, A2	Address Inputs
VSS	Ground
SDA	Data I/O
SCL	Clock Input
WP	Write Protect
VCC	Power Input

1432K Smart Serial EEPROM – 24C32

14.1 General Description

The Microchip Technology Inc. 24C32 is a 4K x 8 (32K bit) Serial Electrically Erasable PROM. This device has been developed for advanced, low power applications such as personal communications or data acquisition. The 24C32 features an input cache for fast write loads with a capacity of eight 8-byte pages, or 64 bytes. It also features a fixed 4K-bit block of ultra-high endurance memory for data that changes frequently. The 24C32 is capable of both random and sequential reads up to the 32K boundary. Functional address lines allow up to eight 24C32 devices on the same bus, for up to 256K bits address space. Advanced CMOS technology makes this device ideal for low-power non-volatile code and data applications. The 24C32 is available in the standard 8-pin plastic DIP and 8-pin surface mount SOIC package.

14.2 Features

- Voltage operating range: 4.5V to 5.5V
- Peak write current 3 mA at 5.5V
- Maximum read current 150 µA at 5.5V
- Standby current 1 µA typical
- Industry standard two-wire bus protocol, I2C compatible
- Including 100 kHz and 400 kHz modes
- Self-timed write cycle (including auto-erase)
- Power on/off data protection circuitry
- Endurance: 10,000,000 Erase/Write cycles guaranteed for High Endurance Block, 1,000,000 E/W cycles guaranteed for Standard Endurance Block
- 8 byte page, or byte modes available
- 1 page x 8 line input cache (64 bytes) for fast write loads

- Schmitt trigger, filtered inputs for noise suppression
- Output slope control to eliminate ground bounce
- 2 ms typical write cycle time, byte or page
- Up to 8 chips may be connected to the same bus for up to 256K bits total memory
- Electrostatic discharge protection > 4000V
- Data retention > 200 years
- 8-pin PDIP/SOIC packages
- Temperature ranges: Commercial (C): 0°C to +70°C, Industrial (I): -40°C to +85°C

11.3 Absolute Maximum Ratings and Electrical Characteristics

VCC 7.0V
All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V
Storage temperature .....-65°C to +150°C
Ambient temp. with power applied .....-65°C to +125°C
Soldering temperature of leads (10 seconds) .....+300°C
ESD protection on all pins .....≥ 4 kV

DC CHARACTERISTICS

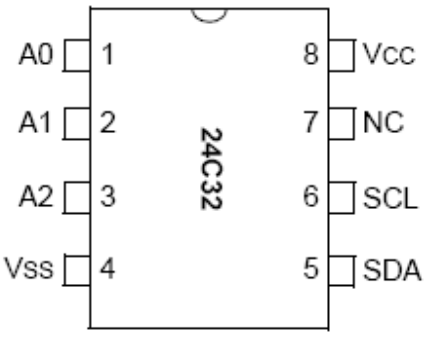
					VCC = +4.5V to +5.5V Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C
Parameter	**Symbol**	**Min**	**Max**	**Units**	**Conditions**
A0, A1, A2, SCL and SDA pins:					
High level input voltage	VIH	.7 Vcc	—	V	
Low level input voltage	VIL	—	.3 Vcc	V	
Hysteresis of Schmitt Trigger inputs	VHYS	.05 Vcc	—	V	(Note)
Low level output voltage	VOL	—	.40	V	IOL = 3.0 mA
Input leakage current	ILI	-10	10	µA	VIN = .1V TO VCC
Output leakage current	ILO	-10	10	µA	VOUT = .1V to VCC
Pin capacitance (all inputs/outputs)	CIN, COUT	—	10	pF	VCC = 5.0V (Note) Tamb = 25°C, Fclk = 1 MHz
Operating current	ICC WRITE ICC Read	— —	3 150	mA µA	VCC = 5.5V, SCL = 400 kHz VCC = 5.5V, SCL = 400 kHz
Standby current	ICCS	—	5	µA	VCC = 5.5V, SCL = SDA = VCC A0, A1, A2 = VSS

AC CHARACTERISTICS

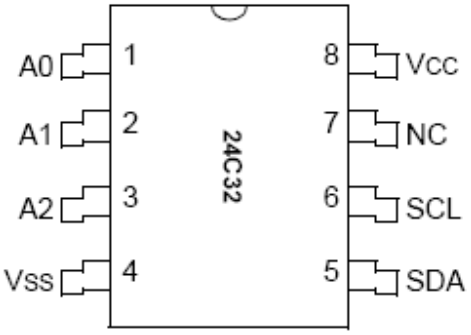
Parameter	Symbol	STD. MODE		FAST MODE		Units	Remarks
		Min	Max	Min	Max		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH min to VIL max	TOF	—	250	20 + 0.1 CB	250	ns	(Note 1), CB ≤ 100 pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Note 3)
Write cycle time	TWR	—	5	—	5	ms/page	(Note 4)
Endurance High Endurance Block Rest of Array	 — —	 10M 1M	 — —	 10M 1M	 — —	 cycles	 25°C, Vcc = 5.0V, Block Mode (Note 5)

11.4 Pinning

PDIP



SOIC



Name	Function
A0,A1,A2	User Configurable Chip Selects
Vss	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
Vcc	+4.5V to 5.5V Power Supply
NC	**No Internal Connection**

15512K CMOS Serial Flash – MX25L512

15.1 General Description

The MX25L512 is a CMOS 524,288 bit serial Flash memory, which is configured as 65,536 x 8 internally. The MX25L512 feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by CS# input. The MX25L512 provide sequential read operation on whole chip. After program/erase command is issued, auto program/ erase algorithms which program/ erase and verify the specified page or sector/block locations will be executed. Program command is executed on page (256 bytes) basis, and erase command is executes on chip or sector (4K-bytes). To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit. When the device is not in operation and CS# is high, it is put in standby mode and draws less than 10uA DC current. The MX25L512 utilize MXIC's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

15.2 Features

GENERAL

- Serial Peripheral Interface (SPI) compatible -- Mode 0 and Mode 3
- 524,288 x 1 bit structure
- 16 Equal Sectors with 4K byte each
- Any Sector can be erased individually
- Single Power Supply Operation
- 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is from 1.5V to 2.5V

PERFORMANCE

- High Performance
- Fast access time: 85MHz serial clock (15pF + 1TTL Load) and 66MHz serial clock (30pF + 1TTL Load)
- Fast program time: 1.4ms(typ.) and 5ms(max.)/page (256-byte per page)
- Fast erase time: 60ms(typ.) and 120ms(max.)/sector (4K-byte per sector) ; 1s(typ.) and 2s(max.)/chip(512Kb)
- Low Power Consumption
- Low active read current: 12mA(max.) at 85MHz, 8mA(max.) at 66MHz and 4mA(max.) at 33MHz
- Low active programming current: 15mA (max.)
- Low active erase current: 15mA (max.)
- Low standby current: 10uA (max.)
- Deep power-down mode 1uA (typical)
- Minimum 100,000 erase/program cycles

SOFTWARE FEATURES

- Input Data Format
- 1-byte Command code
- Block Lock protection
- The BP0~BP1 status bit defines the size of the area to be software protected against Program and Erase instructions.
- Auto Erase and Auto Program Algorithm
- Automatically erases and verifies data at selected sector
- Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
- Electronic Identification
- JEDEC 2-byte Device ID
- RES command, 1-byte Device ID

HARDWARE FEATURES

- SCLK Input
- Serial clock input
- SI Input
- Serial Data Input
- SO Output
- Serial Data Output
- WP# pin
- Hardware write protection
- HOLD# pin pause the chip without diselecting the chip
- PACKAGE
- 8-pin SOP (150mil)
- All Pb-free devices are RoHS Compliant

11.3 Absolute Maximum Ratings

Supply voltage range	V_P		1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ.	3,2	mA
Bridge tied load application (BTL)				
Output power at R_L = 32 Ω				
V_P = 3 V; d_{tot} = 10%	P_o	typ.	140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max.	70	mV
Noise output voltage (r.m.s. value)				
at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	140	µV
Stereo application				
Output power at R_L = 32 Ω				
d_{tot} = 10%; V_P = 3 V	P_o	typ.	35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ.	75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ.	40	dB
Noise output voltage (r.m.s. value)				
at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	100	µV

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig.1		
Storage temperature range	T_{stg}	–55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration			
at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig.4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\|\Delta V\|$	–	–	70	mV
Input impedance (at R_S = ∞)	$\|Z_i\|$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig.5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\|Z_i\|$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

16IC DESCRIPTIONS

16.1 LM1117

16.1.1 General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to as-sure output voltage accuracy to within ±1%. The LM1117 series is available in SOT- 223, TO-220, and TO-252 D-PAK packages. A minimum of 10μF tantalum capacitor is required at the output to improve the transient response and stability.

16.1.2 Features

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 Package
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
- LM1117 0°C to 125°C
- LM1117I -40°C to 125°C

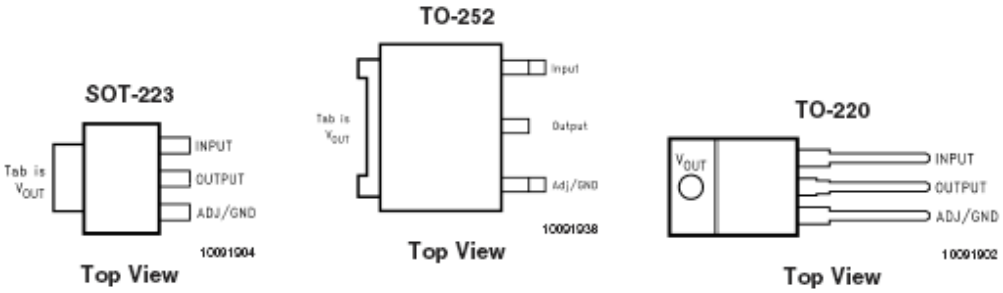
16.1.3 Applications

- 2.85V Model for SCSI-2 Active Termination
- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators 15
- 32" TFT TV Service Manual 10/01/2005
- Battery Charger
- Battery Powered Instrumentation

16.1.4 Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
DC Input Voltage	V_{IN}		7	V
Lead Temperature (Soldering, 5 Seconds)	T_{SOL}		260	℃
Storage Temperature Range	T_{STG}	−65	150	℃
Operating Junction Temperature Range	T_{OPR}	0	125	℃

16.1.5 Pinning



16.2 74HCT4053

16.2.1 General Description

The 74HC4053; 74HCT4053 is a high-speed Si-gate CMOS device and is pin compatible with the HEF4053B. It is specified in compliance with JEDEC standard no. 7A. The 74HC4053; 74HCT4053 is triple 2-channel analog multiplexer/demultiplexer with a common enable input (E). Each multiplexer/demultiplexer has two independent inputs/outputs (nY0 and nY1), a common input/output (nZ) and three digital select inputs (Sn). With E LOW, one of the two switches is selected (low-impedance ON-state) by S1 to S3. With E HIGH, all switches are in the high-impedance OFF-state, independent of S1 to S3. VCC and GND are the supply voltage pins for the digital control inputs (S1 to S3 and E). The VCC to GND ranges are 2.0 V to 10.0 V for 74HC4053 and 4.5 V to 5.5 V for 74HCT4053. The analog inputs/outputs (nY0 and nY1, and nZ) can swing between VCC as a positive limit and VEE as a negative limit. VCC - VEE may not exceed 10.0 V.
For operation as a digital multiplexer/demultiplexer, VEE is connected to GND (typically ground).

16.2.2 Features

- Low ON resistance:
- 80 W (typical) at VCC - VEE = 4.5 V
- 70 W (typical) at VCC - VEE = 6.0 V
- 60 W (typical) at VCC - VEE = 9.0 V
- Logic level translation:
- To enable 5 V logic to communicate with ±5 V analog signals
- Typical ‘break before make’ built in
- Complies with JEDEC standard no. 7A
- ESD protection: HBM EIA/JESD22-A114-C exceeds 2000 V, MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

16.2.3 Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

16.2.4 Absolute Maximum Ratings

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+11.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V		-	±20	mA
I_{SK}	switch clamping current	$V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V		-	±20	mA
Symbol	**Parameter**	**Conditions**		**Min**	**Max**	**Unit**
I_S	switch current	-0.5 V < V_S < V_{CC} + 0.5 V		-	±25	mA
I_{EE}	negative supply current			-	−20	mA
I_{CC}	quiescent supply current			-	50	mA
I_{GND}	ground current			-	−50	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to + 125 °C				
	DIP16 package		[2]	-	750	mW
	SO16 package		[3]	-	500	mW
	SSOP16 package		[4]	-	500	mW
	TSSOP16 package		[4]	-	500	mW
	DHVQFN16 package		[5]	-	500	mW
P_S	power dissipation per switch			-	100	mW

16.2.5 Pinning

Symbol	Pin	Description
2Y1	1	2 independent input/output 1
2Y0	2	2 independent input/output 0
3Y1	3	3 independent input/output 1
3Z	4	3 common input/output
3Y0	5	3 independent input/output 0
$\overline{E}$	6	enable input (active LOW)
V_{EE}	7	negative supply voltage
GND	8	ground (0 V)
S3	9	select input 3
S2	10	select input 2
S1	11	select input 1
1Y0	12	1 independent input/output 0
1Y1	13	1 independent input/output 1
1Z	14	1 common input/output
2Z	15	2 common input/output
V_{CC}	16	supply voltage

16.3 NUP4004M5

16.3.1 General Description

This 5-Pin bi-directional transient suppressor array is designed for applications requiring transient overvoltage protection capability. It is intended for use in transient voltage and

ESD sensitive equipment such as computers, printers, cell phones, medical equipment, and other applications. Its integrated design provides bi-directional protection for four separate lines using a single TSOP-5 package. This device is ideal for situations where board space is a premium.

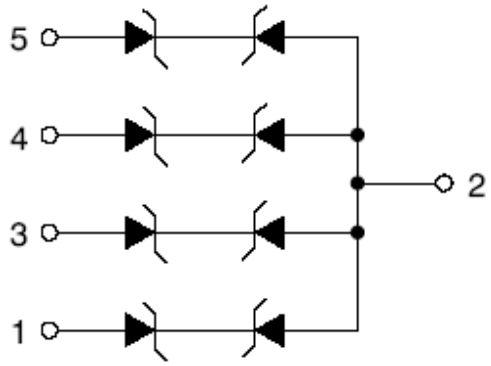
16.3.2 Features

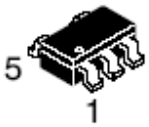
- Bi-directional Protection for Four Lines in a Single TSOP-5 Package
- Low Leakage Current
- Low Capacitance
- Provides ESD Protection for JEDEC Standards JESD22
- Machine Model = Class C
- Human Body Model = Class 3B
- Provides ESD Protection for IEC 61000-4-2, 15 kV (Air), 8 kV (Contact)
- This is a Pb-Free Device

16.3.3 Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−40 to 125	°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
Lead Solder Temperature – Maximum (10 sec)	T_L	260	°C
Human Body Model (HBM) Machine Model (MM) IEC 61000−4−2 Air (ESD) IEC 61000−4−2 Contact (ESD)	ESD	16 0.4 30 30	kV

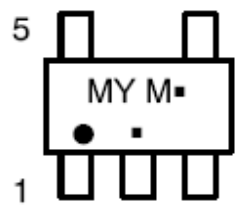
16.3.4 Pinning





TSOP−5
CASE 483

MARKING DIAGRAM



16.4 FDN336P

16.4.1 General Description

The ST24LC21 is a 1K bit electrically erasable programmable memory (EEPROM), organized by 8 bits.This device can operate in two modes: Transmit Only mode and I2C bidirectional mode. When powered, the device is in Transmit Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK. The device will switch to the I2C bidirectional mode upon the falling edge of the signal applied on SCL pin. The ST24LC21 cannot switch from the I2C bidirectional mode to the Transmit Only mode (except when the power supply is removed). The device operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

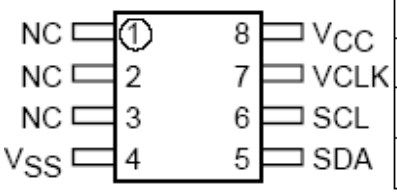
16.4.2 Features

- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- 2.5V to 5.5V SINGLE SUPPLY VOLTAGE
- 400k Hz COMPATIBILITY OVER the FULL RANGE of SUPPLY VOLTAGE
- TWO WIRE SERIAL INTERFACE I2C BUS COMPATIBLE
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES

16.4.3 Absolute Maximum Ratings

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature		grade 1	0 to 70	°C
T_{STG}	Storage Temperature			–65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8 package) (PSDIP8 package)	40 sec 10 sec	215 260	°C
V_{IO}	Input or Output Voltages			–0.3 to 6.5	V
V_{CC}	Supply Voltage			–0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) (2)			4000	V
	Electrostatic Discharge Voltage (Machine model) (3)			500	V

16.4.4 Pinning



SDA	Serial Data Address Input/Output
SCL	Serial Clock (I^2C mode)
V_{CC}	Supply Voltage
V_{SS}	Ground
VCLK	Clock Transmit only mode

16.5 TL062 -

16.5.1 General Description

Low-power JFET-input operational amplifier

16.5.2 Features

- Very Low Power Consumption
- Typical Supply Current . . . 200 µA (Per Amplifier)
- Wide Common-Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Common-Mode Input Voltage Range Includes VCC+
- Output Short-Circuit Protection
- High Input Impedance . . . JFET-Input Stage
- Internal Frequency Compensation
- Latch-Up-Free Operation
- High Slew Rate . . . 3.5 V/µs Typ

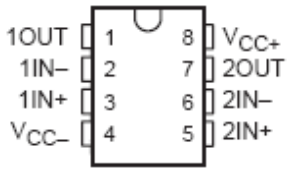
16.5.3 Absolute Maximum Ratings

		TL06_C TL06_AC TL06_BC	TL06_I	TL06_M	UNIT
Supply voltage, V_{CC+} (see Note 1)		18	18	18	V
Supply voltage, V_{CC-} (see Note 1)		–18	–18	–18	V
Differential input voltage, V_{ID} (see Note 2)		±30	±30	±30	V
Input voltage, V_I (see Notes 1 and 3)		±15	±15	±15	V
Duration of output short circuit (see Note 4)		Unlimited	Unlimited	Unlimited	
Package thermal impedance, θ_{JA} (see Notes 5 and 6)	D (8-pin) package	97	97		°C/W
	D (14-pin) package	86	86		
	N package	80	80		
	NS package	76	76		
	P package	85	85		
	PS package	95	95		
	PW (8-pin) package	149	149		
	PW (14-pin) package	113	113		
Package thermal impedance, θ_{JC} (see Notes 7 and 8)	FK package			5.61	°C/W
	J package			15.05	
	JG package			14.5	
	W package			14.65	
Operating virtual junction temperature, T_J		150	150	150	°C
Case temperature for 60 seconds	FK package			260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	J, JG, U, or W package			300	°C
Lead temperature 1,6 mm (1/6 inch) from case for 10 seconds	D, N, NS, P, PS, or PW package	260	260		°C
Storage temperature range, T_{stg}		–65 to 150	–65 to 150	–65 to 150	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. All voltage values except differential voltages are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
6. The package thermal impedance is calculated in accordance with JESD 51-7.
7. Maximum power dissipation is a function of $T_J(max)$, θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) – T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
8. The package thermal impedance is calculated in accordance with MIL-STD-883.

16.5.4 Pinning



16.6 PI5V330

16.6.1 General Description

Pericom Semiconductor.s PI5V series of mixed signal video circuits are produced in the Company.s advanced CMOS low-power technology, achieving industry leading performance. The PI5V330 is a true bidirectional Quad 2-channel multiplexer/demultiplexer that is recommended for both RGB and composite video switching applications. The VideoSwitch. can be driven from a current output RAMDAC or voltage output composite video source. Low ON-resistance and wide bandwidth make it ideal for video and other applications. Also this device has exceptionally high current capability which is far greater than most analog switches offered today. A single 5V supply is all that is required for operation. The PI5V330 offers a high-performance, low-cost solution to switch between video sources. The application section describes the PI5V330 replacing the HC4053 multiplier and buffer/amplifier.

16.6.2 Features

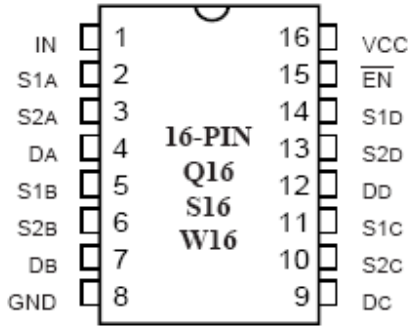
- High-performance, low-cost solution to switch between video sources
- Wide bandwidth: 200 MHz
- Low ON-resistance: 3Ω
- Low crosstalk at 10 MHz: .58 dB
- Ultra-low quiescent power (0.1 µA typical)
- Single supply operation: +5.0V
- Fast switching: 10 ns
- High-current output: 100 mA
- Packages available:
- 16-pin 300-mil wide plastic SOIC (S)
- 16-pin 150-mil wide plastic SOIC (W)
- 16-pin 150-mil wide plastic QSOP (Q)

16.6.3 Absolute Maximum Ratings

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

16.6.4 Pinning



Pin Name	Description
$S1_A$, $S2_A$ $S1_B$, $S2_B$ $S1_C$, $S2_C$ $S1_D$, $S2_D$	Analog Video I/O
IN	Select Input
$\overline{EN}$	Enable
D_A, D_B, D_C, D_D	Analog Video I/O
GND	Ground
V_{CC}	Power

16.7 AZC099-04S

16.7.1 General Description

AZC099-04S is a high performance and low cost design which includes surge rated diode arrays to protect high speed data interfaces. The AZC099-04S family has been specifically designed to protect sensitive components, which are connected to data and transmission lines, from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Lightning.

AZC099-04S is a unique design which includes surge rated, low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the power supply line or to the ground line. The internal unique design of clamping cell prevents over-voltage on the power line, protecting any downstream components.

AZC099-04S may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (± 15kV air, ±8kV contact discharge).

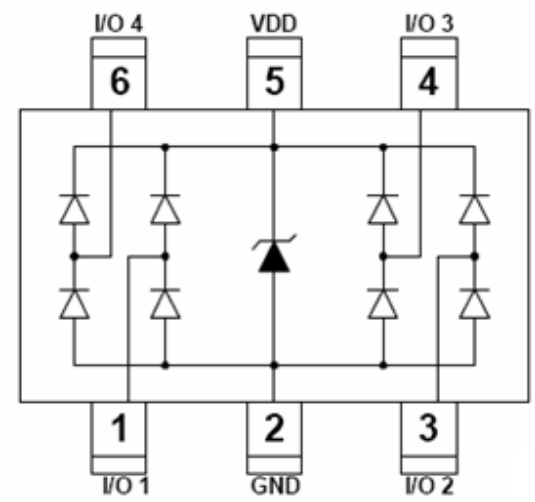
16.7.2 Features

- ESD Protect for 4 high-speed I/O channels
- Provide ESD protection for each channel to IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact) IEC 61000-4-4 (EFT) (5/50ns) Level-3, 20A for I/O, 40A for Power IEC 61000-4-5 (Lightning) 4A (8/20μs)
- 5V operating voltage □□ Low capacitance : 1.0pF typical
- Fast turn-on and Low clamping voltage
- Array of surge rated diodes with internal equivalent TVS diode
- Small package saves board space
- Solid-state silicon-avalanche and active circuit triggering technology

16.7.3 Absolute Maximum Ratings

PARAMETER	PARAMETER	RATING	UNITS
Peak Pulse Current (tp =8/20μs)	I_{PP}	5.5	A
Operating Supply Voltage (VDD-GND)	V_{DC}	6	V
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	15 8	kV
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	°C
Operating Temperature	T_{OP}	-55 to +85	°C
Storage Temperature	T_{STO}	-55 to +150	°C
DC Voltage at any I/O pin	V_{IO}	(GND – 0.5) to (VDD + 0.5)	V

16.7.4 Pinning



16.8 TDA1308

16.8.1 General Description

The TDA1308; TDA1308A is an integrated class-AB stereo headphone driver contained in an SO8, DIP8 or a TSSOP8 plastic package. The TDA1308AUK is available in an 8 bump wafer level chip-size package (WLCSP8). The device is fabricated in a 1 mm Complementary Metal Oxide Semiconductor (CMOS) process and has been primarily developed for portable digital audio applications. The difference between the TDA1308 and the TDA1308A is that the TDA1308A can be used at low supply voltages.

16.8.2 Features

- Wide temperature range
- No switch ON/OFF clicks
- Excellent power supply ripple rejection
- Low power consumption
- Short-circuit resistant
- High performance
- High signal-to-noise ratio

- High slew rate
- Low distortion
- Large output voltage swing

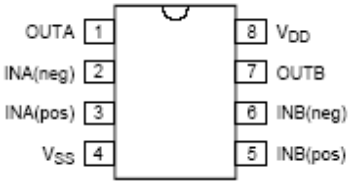
16.8.3 Absolute Maximum Ratings

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			0	8.0	V
$t_{SC(O)}$	output short-circuit duration	T_{amb} = 25 °C; P_{tot} = 1 W		20	-	s
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
V_{esd}	electrostatic discharge voltage	HBM	[1]	−2	+2	kV
		MM	[2]	−200	+200	V

[1] Human body model (HBM): C = 100 pF; R = 1500 Ω; 3 pulses positive plus 3 pulses negative.

[2] Machine model (MM): C = 200 pF; L = 0.5 mH; R = 0 Ω; 3 pulses positive plus 3 pulses negative.

16.8.4 Pinning



Symbol	Pin	Description
OUTA	1	output A
INA(neg)	2	inverting input A
INA(pos)	3	non-inverting input A
V_{SS}	4	negative supply
INB(pos)	5	non-inverting input B

16.9 LM358D

16.9.1 General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies. The LM358 and LM2904 are available in a chip sized package (8-Bump micro SMD) using National's micro SMD package technology.

16.9.2 Features

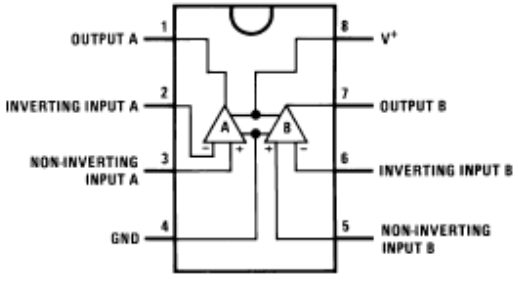
- Available in 8-Bump micro SMD chip sized package,
- Internally frequency compensated for unity gain
- Large dc voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz (temperature compensated)
- Wide power supply: Single supply: 3V to 32V or dual supplies: ±1.5V to ±16V

- Low supply current drain (500 µA)—essentially independent of supply voltage
- Low input offset voltage: 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing

16.9.3 Absolute Maximum Ratings

	LM158/LM258/LM358 LM158A/LM258A/LM358A
Supply Voltage, V^+	32V
Differential Input Voltage	32V
Input Voltage	–0.3V to +32V
Power Dissipation (Note 1)	
Molded DIP	830 mW
Metal Can	550 mW
Small Outline Package (M)	530 mW
micro SMD	435mW
Output Short-Circuit to GND	
(One Amplifier) (Note 2)	
$V^+ \leq 15V$ and $T_A = 25^\circ C$	Continuous
Input Current ($V_{IN} < -0.3V$) (Note 3)	50 mA
Operating Temperature Range	
LM358	0°C to +70°C
LM258	–25°C to +85°C
LM158	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature, DIP	
(Soldering, 10 seconds)	260°C
Lead Temperature, Metal Can	
(Soldering, 10 seconds)	300°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods surface mount devices.	
ESD Tolerance (Note 10)	250V

16.9.4 Pinning



16.10 74LCX244

16.10.1 General Description

The LCX244 contains eight non-inverting buffers with 3-STATE outputs. The device may be employed as a memory address driver, clock driver and bus-oriented

transmitter/receiver. The LCX244 is designed for low voltage (2.5V or 3.3V) VCC applications with capability of interfacing to a 5V signal environment. The LCX244 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

16.10.2 Features

- 5V tolerant inputs and outputs
- 2.3V to 3.6V VCC specifications provided
- 6.5ns Tpd max. (VCC=3.3V), 10µA ICCmax.
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- ±24mA output drive (VCC=3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500mA
- ESD performance:Human body model>2000V, Machine model>200V
- Leadless DQFN package

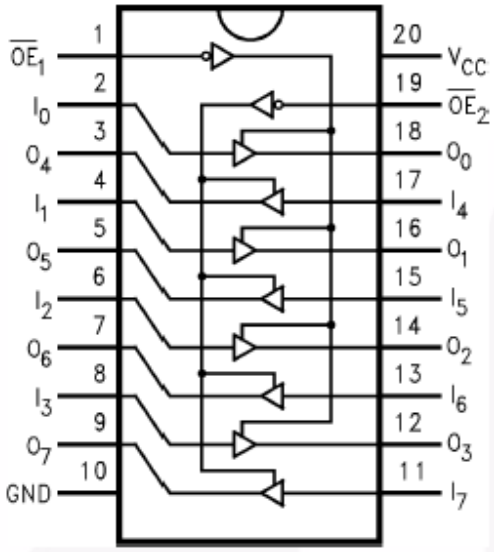
16.10.3 Absolute Maximum Ratings

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_I	DC Input Voltage	–0.5V to +7.0V
V_O	DC Output Voltage Output in 3-STATE	–0.5V to +7.0V
	Output in HIGH or LOW State(3)	–0.5V to V_{CC} + 0.5V
I_{IK}	DC Input Diode Current, V_I < GND	–50mA
I_{OK}	DC Output Diode Current V_O < GND	–50mA
	V_O > V_{CC}	+50mA
I_O	DC Output Source/Sink Current	±50mA
I_{CC}	DC Supply Current per Supply Pin	±100mA
I_{GND}	DC Ground Current per Ground Pin	±100mA
T_{STG}	Storage Temperature	–65°C to +150°C

Note:

3. I_O Absolute Maximum Rating must be observed.

16.10.4 Pinning



Inputs		Outputs
$\overline{OE}_1$	I_n	(Pins 12, 14, 16, 18)
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
$\overline{OE}_2$	I_n	(Pins 3, 5, 7, 9)
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

16.11 74LCX245

16.11.1 General Description

The LCX245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V and 3.3V) VCC applications with capability of interfacing to a 5V signal environment. The T/R input determines the direction of data flow through the device. The OE input disables both the A and B ports by placing them in a high impedance state.
The LCX245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

16.11.2 Features

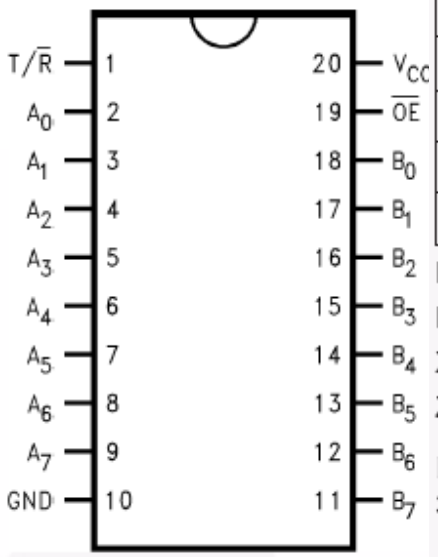
- 5V tolerant inputs and outputs
- 2.3V to 3.6V VCC specifications provided
- 7.0ns tPDmax. (VCC=3.3V), 10µA ICCmax.
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- ±24mA output drive (VCC=3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500mA
- ESD performance: Human body model>2000V, Machine model>200V
- Leadless DQFN package

16.11.3 Absolute Maximum Ratings

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_I	DC Input Voltage	–0.5V to +7.0V
V_O	DC Output Voltage	
	Output in 3-STATE	–0.5V to +7.0V
	Output in HIGH or LOW State(4)	–0.5V to V_{CC} + 0.5V
I_{IK}	DC Input Diode Current, V_I < GND	–50mA
I_{OK}	DC Output Diode Current	
	V_O < GND	–50mA
	V_O > V_{CC}	+50mA
I_O	DC Output Source/Sink Current	±50mA
I_{CC}	DC Supply Current per Supply Pin	±100mA
I_{GND}	DC Ground Current per Ground Pin	±100mA
T_{STG}	Storage Temperature	–65°C to +150°C

Note:
4. I_O Absolute Maximum Rating must be observed.

16.11.4 Pinning



Inputs		Outputs
OE	T/R	
L	L	Bus B_0 – B_7 Data to Bus A_0 – A_7
L	H	Bus A_0 – A_7 Data to Bus B_0 – B_7
H	X	HIGH Z State on A_0 – A_7, B_0 – B_7(3)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Note:
3. Unused bus terminals during HIGH Z State must be held HIGH or LOW.

16.12 FSA3157

16.12.1 General Description

The NC7SB3157 / FSA3157 is a high-performance, single- pole / double-throw (SPDT) analog switch or 2:1 multiplexer/ de-multiplexer bus switch. The device is fabricated with advanced sub-micron CMOS technology to achieve high-speed enable and disable times and low on resistance. The break-beforemake select circuitry prevents disruption of signals on the B Port due to both switches temporarily being enabled during select pin

switching. The device is specified to operate over the 1.65 to 5.5V VCC operating range. The control input tolerates voltages up to 5.5V, independent of the VCC operating range.

16.12.2 Features

- Useful in both analog and digital applications
- Space-saving, SC70 6-lead surface mount package
- Ultra-small, MicroPak™ Pb-free leadless package
- Low On Resistance: <10Ω on typical at 3.3V VCC
- Broad VCC operating range: 1.65V to 5.5V
- Rail-to-rail signal handling
- Power-down, high-impedance control input
- Over-voltage tolerance of control input to 7.0V
- Break-before-make enable circuitry
- 250 MHz, 3dB bandwidth

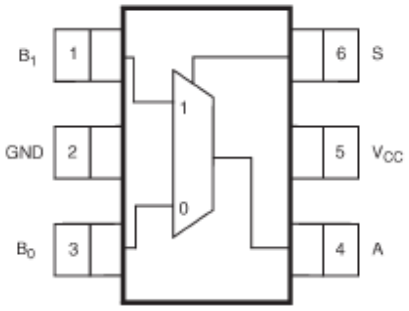
16.12.3 Absolute Maximum Ratings

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_S	DC Switch Voltage[1]	–0.5V to V_{CC} +0.5V
V_{IN}	DC Input Voltage[1]	–0.5V to +7.0V
I_{IK}	DC Input Diode Current at V_{IN} < 0V	–50mA
I_{OUT}	DC Output Current	128mA
I_{CC}/I_{GND}	DC V_{CC} or Ground Current	±100mA
T_{STG}	Storage Temperature Range	–65°C to +150°C
T_J	Junction Temperature Under Bias	150°C
T_L	Junction Lead Temperature (Soldering, 10 seconds)	260°C
P_D	Power Dissipation at +85°C	180mW
ESD	Electrostatic Discharge, Human Body Model	4000V

Note:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

16.12.4 Pinning



Pin Names	Description
A, B_0, B_1	Data Ports
S	Control Input

16.13 TSH343

16.13.1 General Description

The TSH343 is a triple single-supply video buffer featuring an internal gain of 6dB and a large bandwidth of 280MHz. The main advantage of this circuit is that its input DC level shifter allows for video signals on 75Ω video lines without damage to the synchronization tip of the video signal, while using a single 5V power supply with no input capacitor. The DC level shifter is internally fixed and optimized to keep the output video signals between low and high output rails in the best position for the greatest linearity. Chapter 4 of this datasheet gives technical support when using the TSH343 as Y-Pb-Pr driver for video DAC output on a video line (see TSH344 for RGB signals). The TSH343 is available in the compact SO8 plastic package for optimum space-saving.

16.13.2 Features

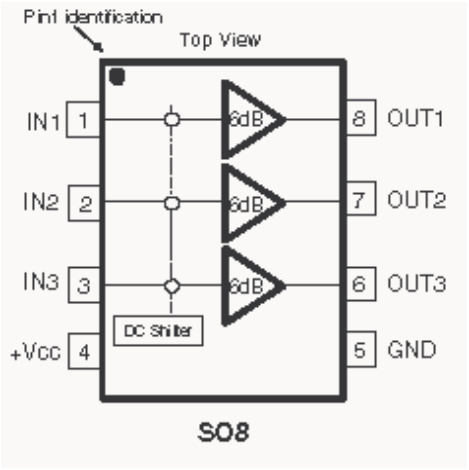
- Bandwidth: 280MHz
- 5V single-supply operation
- Internal input DC level shifter
- No input capacitor required
- Internal gain of 6dB for a matching between 3 channels
- AC or DC output-coupled
- Very low harmonic distortion
- Slew rate: 780V/µs
- Specified for 150Ω and 100Ω loads
- Tested on 5V power supply
- Data min. and max. are tested during production

16.13.3 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_{in}	Input Voltage Range (2)	0 to +1.4	V
T_{oper}	Operating Free Air Temperature Range	-40 to +85	°C
T_{std}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thjc}	SO8 Thermal Resistance Junction to Case	28	°C/W
R_{thja}	SO8 Thermal Resistance Junction to Ambient Area	157	°C/W
$P_{max.}$	Maximum Power Dissipation (@Ta=25°C) for Tj=150°C	800	mW
ESD	CDM: Charged Device Model HBM: Human Body Model MM: Machine Model	2 1.5 200	kV kV V

1. All voltage values, except differential voltage, are with respect to network terminal.
2. The magnitude of input and output voltage must never exceed V_{CC} +0.3V.

16.13.4 Pinning



16.14 MT48LC4M16A2TG8E

16.14.1 General Description

The 64Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 67,108,864 bits. It is internally configured as a quad-bank DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the x4's 16,777,216-bit banks is organized as 4,096 rows by 1,024 columns by 4 bits. Each of the x8's 16,777,216-bit banks is organized as 4,096 rows by 512 columns by 8 bits. Each of the x16's 16,777,216-bit banks is organized as 4,096 rows by 256 columns by 16 bits. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then ollowed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row).

16.14.2 Features

- PC66-, PC100- and PC133-compliant
- 143 MHz, graphical 4 Meg x 16 option
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge, includes CONCURRENT AUTO PRECHARGE, and AutO Refresh Modes
- Self Refresh Modes: standard and low power
- 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Single +3.3V ±0.3V power supply

16.14.3 Absolute Maximum Ratings

Voltage on V_{DD}, $V_{DD}Q$ Supply
Relative to Vss ..... -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to Vss ..... -1V to +4.6V
Operating Temperature,
T_A (commercial) ..... 0°C to +70°C
Operating Temperature,
T_A (industrial) ..... -40°C to +85°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W

16.14.4 Pinning

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
38	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
37	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
19	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
16, 17, 18	WE#, CAS#, RAS#	Input	Command Inputs: WE#, CAS# and RAS# (along with CS#) define the command being entered.
39	x4, x8: DQM	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. On the x4 and x8, DQML (Pin 15) is a NC and DQMH is DQM. On the x16, DQML corresponds to DQ0-DQ7 and DQMH corresponds to DQ8-DQ15. DQML and DQMH are considered same state when referenced as DQM.
15, 39	x16: DQML, DQMH		
20, 21	BA0, BA1	Input	Bank Address Inputs: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
23-26, 29-34, 22, 35	A0-A11	Input	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (column-address A0-A9 [x4]; A0-A8 [x8]; A0-A7 [x16]; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2, 4, 5, 7, 8, 10, 11, 13, 42, 44, 45, 47, 48, 50, 51, 53	DQ0-DQ15	x16: I/O	Data Input/Output: Data bus for x16 (4, 7, 10, 13, 42, 45, 48, 51 are NCs for x8; and 2, 4, 7, 8, 10, 13, 42, 45, 47, 48, 51, 53 are NCs for x4).
2, 5, 8, 11, 44, 47, 50, 53	DQ0-DQ7	x8: I/O	Data Input/Output: Data bus for x8 (2, 8, 47, 53 are NCs for x4).
5, 11, 44, 50	DQ0-DQ3	x4: I/O	Data Input/Output: Data bus for x4.
36, 40	NC	–	No Connect: These pins should be left unconnected.
3, 9, 43, 49	VccQ	Supply	DQ Power: Isolated DQ power on the die for improved noise immunity.
6, 12, 46, 52	VssQ	Supply	DQ Ground: Isolated DQ ground on the die for improved noise immunity.
1, 14, 27	Vcc	Supply	Power Supply: +3.3V ±0.3V.
28, 41, 54	Vss	Supply	Ground.

16.15 MP1583

16.15.1 General Description

The MP1583 is a step-down regulator with a built in internal Power MOSFET. It achieves 3A continuous output current over a wide input supply range with excellent load and line regulation.
Current mode operation provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.
Adjustable soft-start reduces the stress on the input source at turn-on. In shutdown mode the regulator draws 20μA of supply current.
The MP1583 requires a minimum number of readily available external components to complete a 3A step down DC to DC converter solution.

16.15.2 Features

- 3A Output Current
- Programmable Soft-Start
- 100mΩ Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 20μA Shutdown Mode
- Fixed 385KHz frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.75 to 23V operating Input Range
- Output Adjustable From 1.22 to 21V
- Under Voltage Lockout
- Available in 8 pin SOIC Package
- 3A Evaluation Board Available

16.15.3 Absolute Maximum Ratings

Supply Voltage V_{IN}	-0.3V to 28V
Switch Voltage V_{SW}	-1V to V_{IN}+0.3V
Boost Voltage V_{BS}	V_{SW}-0.3V to V_{SW}+6V
All Other Pins	-0.3V to 6V
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to 150°C

16.15.4 Pinning

#	Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side n-channel MOSFET switch. Connect a 4.7nF or greater capacitor from SW to BS to power the high side switch.
2	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 23V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See *Input Capacitor*
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground. (Note: Connect the exposed pad on backside to Pin 4).
5	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 1.222V. See *Setting the Output Voltage*
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required. See *Compensation*
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. For automatic startup, leave EN unconnected.
8	SS	Soft Start Control Input. SS controls the soft start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1µF capacitor sets the soft-start period to 10ms. To disable the soft-start feature, leave SS unconnected.

16.16 MP2112

16.16.1 General Description

The MP2112 is a 1MHz constant frequency, current mode, PWM step-down converter. The device integrates a main switch and a synchronous rectifier for high efficiency without an external Schottky diode. It is ideal for powering portable equipment that powered by a single cell Lithium-Ion (Li+) battery. The MP2112 can supply 1A of load current from a 2.5V to 6V input voltage. The output voltage can be regulated as low as 0.6V. The MP2112 can also run at 100% duty cycle for low dropout applications.
The MP2112 is available in a space-saving 6-pin QFN package.

16.16.2 Features

- High Efficiency: Up to 95%
- 1MHz Constant Switching Frequency
- 1A Available Load Current
- 2.5V to 6V Input Voltage Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- Current Mode Control
- Short Circuit Protection
- Thermal Fault Protection
- <0.1µA Shutdown Current
- Space Saving 3mm x 3mm QFN6 Package

16.16.3 Absolute Maximum Ratings

V_{IN} to GND ..... –0.3V to +6.5V
V_{SW} to GND..... –0.3V to V_{IN} +0.3V
V_{FB}, V_{EN} to GND..... –0.3V to +6.5V
Junction Temperature.....+150°C
Lead Temperature .....+260°C
Storage Temperature .....–65°C to +150°C

16.16.4 Pinning

Pin #	Name	Description
1	FB	Feedback Input. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.6V.
2	GND	Ground.
3	SW	Power Switch Output. Inductor connection to drains of the internal PFET and NFET switches.
4	VINB	Supply Input-Power.
5	VINA	Supply Input-Analog.
6	EN	Enable Input.

16.17 MAX809LTR

16.17.1 General Description

The MAX809 and MAX810 are cost-effective system supervisor circuits designed to monitor VCC in digital systems and provide a reset signal to the host processor when necessary. No external components are required. The reset output is driven active within ~200msec of VCC falling through the reset voltage threshold. Reset is maintained active for a timeout period which is trimmed by the factory after VCC rises above the reset threshold. The MAX810 has an active-high RESET output while the MAX809 has an active-low RESET output. Both devices are available in SOT-23 and SC-70 packages. The MAX809/810 are optimized to reject fast transient glitches on the VCC line. Low supply current of 0.5 A (VCC = 3.2 V) makes these devices suitable for battery powered applications.

16.17.2 Features

- Precision VCC Monitor for 1.5 V, 2.5 V, 3.0 V, 3.3 V, and 5.0 V Supplies
- Precision Monitoring Voltages from 1.2 V to 4.9 V Available in 100 mV Steps
- Four Guaranteed Minimum Power-On Reset Pulse Width Available (1 ms, 20 ms, 100 ms, and 140 ms)
- RESET Output Guaranteed to VCC = 1.0 V.
- Low Supply Current
- Compatible with Hot Plug Applications
- VCC Transient Immunity
- No External Components
- Wide Operating Temperature: -40°C to 105°C
- Pb-Free Packages are Available

16.17.3 Absolute Maximum Ratings

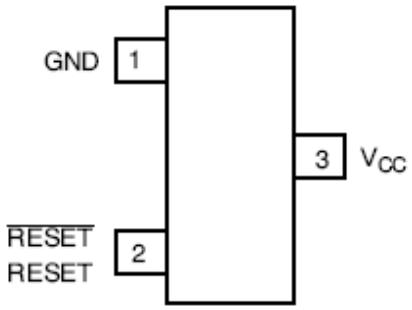
Rating		Symbol	Value	Unit
Power Supply Voltage (V_{CC} to GND)		V_{CC}	-0.3 to 6.0	V
RESET Output Voltage (CMOS)			-0.3 to (V_{CC} + 0.3)	V
Input Current, V_{CC}			20	mA
Output Current, $\overline{RESET}$			20	mA
dV/dt (V_{CC})			100	V/µsec
Thermal Resistance, Junction-to-Air (Note 1)	SOT-23 SC-70	$R_{\theta JA}$	301 314	°C/W
Operating Junction Temperature Range		T_J	-40 to +105	°C
Storage Temperature Range		T_{stg}	-65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)		T_{sol}	+260	°C
ESD Protection Human Body Model (HBM): Following Specification JESD22-A114 Machine Model (MM): Following Specification JESD22-A115			 2000 200	V
Latchup Current Maximum Rating: Following Specification JESD78 Class II Positive Negative		$I_{Latchup}$	 200 200	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This based on a 35x35x1.6mm FR4 PCB with 10mm^2 of 1 oz copper traces under natural convention conditions and a single component characterization.
2. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \quad \text{with } T_{J(max)} = 150°C$$

16.17.4 Pinning



Pin No.	Symbol	Description
1	GND	Ground
2	$\overline{RESET}$ (MAX809)	$\overline{RESET}$ output remains low while V_{CC} is below the reset voltage threshold, and for a reset timeout period after V_{CC} rises above reset threshold
2	RESET (MAX810)	RESET output remains high while V_{CC} is below the reset voltage threshold, and for a reset timeout period after V_{CC} rises above reset threshold
3	V_{CC}	Supply Voltage (Typ)

17SERVICE MENU SETTINGS

In order to reach service menu, First Press **"MENU"** Then press the remote control code, which is **"4725"**. In DTV mode, first press **"MENU**" and select **"TV SETUP"**. Then, press **"4725"**.

17.1 Video Setup

Panel Info <.....>

32_LC_SAC1

Blue Background <.....>

*If "Menu" selected, **"Blue Background"** item is seen in **"Feature"** menu.*

*If "Yes" selected, **"Blue Background"** is on and not seen in **"Feature"** menu*

Film Mode <.....>

*If "Yes" selected, **"**Film Mode**"** feature is active.*

Dynamic Contrast <.....>

*If "Yes" selected, **"**Dynamic Contrast**"** feature is active.*

Game Mode <.....>

*If "Yes" selected, **"**Game Mode**"** feature is active*

SRGB For PC <.....>

If "Yes" selected, PCs can use SRGB option.

Dynamic Noise Reduction<.....>

*If "Yes" selected, **"**Dynamic Noise Reduction**"** feature is active*

WSS Option<.....>

If "Yes" selected, WSS Option can be used

17.2 AudioSetup

BG<.....>

Europe
New Zelland
Australia
No

DK<.....>
I<.....>
L<.....>

Equalizer <.....>

*If "Yes" selected, **"Equalizer"** item is seen in **"Sound"** menu.*

Headphone <.....>

*If "Yes" selected, **"Headphone"** item is seen in **"Sound"** menu.*

Power On/Off Melody <.....>

If "Yes" selected, when power on/off conditions, the power on/off melody can be heard.

Dynamic Bass <.....>*Value between 0 to 12*

Effect<.....> *Value between 0 to 7*

Audio Delay ,offset <.....> *Value between 0 to 190*

Audio Setup Cont...2

Carrier mute<.....> *Value between 0 to 28*

Headphone Sound Select <.....>

Always Active Select

Always Inactive Select

Menu

Always Main Menu

Always PIP/PAP Window

Sound Mode Detect Time <.....> *Value between 0 to 255*

Noise Reduction Threshold <.....> *Value between 0 to 255*

Noise Reduction Time <.....> *Value between 0 to 15*

AVL Attack Time <.....> *Value between 0 to 255*

AVL Release Time <.....> *Value between 0 to 255*

Prescales (AVL On)

FM Prescale<.....> *Value between 0 to 255*

AM Prescale <.....> *Value between 0 to 255*

NICAM Prescale <.....> *Value between 0 to 255*

SCART Prescale <.....> *Value between 0 to 255*

FAV Prescale <.....> *Value between 0 to 255*

DTV Prescale <.....> *Value between 0 to 255*

HDMI Prescale <.....> *Value between 0 to 255*

YPbPr/PC Prescale <.....> *Value between 0 to 255*

An. USB Prescale <.....> *Value between 0 to 255*

Dig. USB Prescale <.....> *Value between 0 to 255*

Prescales (AVL Off)

FM Prescale<.....> *Value between 0 to 255*

AM Prescale <.....> *Value between 0 to 255*

NICAM Prescale <.....> *Value between 0 to 255*

SCART Prescale <.....> *Value between 0 to 255*

FAV Prescale <.....> *Value between 0 to 255*

DTV Prescale <.....> *Value between 0 to 255*

HDMI Prescale <.....> *Value between 0 to 255*

YPbPr/PC Prescale <.....> *Value between 0 to 255*

An. USB Prescale <.....> *Value between 0 to 255*

Dig. USB Prescale <.....> *Value between 0 to 255*

Clipping Levels (AVL On)

FM Clipping <.....> *Value between 0 to 255*

AM Clipping <.....> *Value between 0 to 255*

NICAM Clipping <.....> *Value between 0 to 255*

SCART Clipping <.....> *Value between 0 to 255*

FAV Clipping <.....> *Value between 0 to 255*

DTV Clipping <.....> *Value between 0 to 255*

HDMI Clipping <.....> *Value between 0 to 255*

YPbPr/PC Clipping <.....> *Value between 0 to 255*

An. USB Clipping <.....> *Value between 0 to 255*

Dig. USB Clipping <.....> *Value between 0 to 255*

Clipping Levels (AVL Off)

FM Clipping <.....> *Value between 0 to 255*

AM Clipping <.....> *Value between 0 to 255*

NICAM Clipping <.....> *Value between 0 to 255*

SCART Clipping <.....> *Value between 0 to 255*
FAV Clipping <.....> *Value between 0 to 255*
DTV Clipping <.....> *Value between 0 to 255*
HDMI Clipping <.....> *Value between 0 to 255*
YPbPr/PC Clipping <.....> *Value between 0 to 255*
An. USB Clipping <.....> *Value between 0 to 255*
Dig. USB Clipping <.....> *Value between 0 to 255*

17.3 Service Scan/Tuning Setup

First Search for L/L' <.....>
ATS Delay Time (ms) <.....> *Value between 0 to +200*
Main Tuner Setup
- ***Tuner Type***
  - ***LC_TDTC_GXX1D***
  - ***Thomson DTT7543X***
  - ***Philips TD1318AF-3***
  - ***Samsung DTOs403LH172A***
  - ***Generic (Analog Only)***
    - ***Control Byte <.....>*** *Value between 0 to +255*
    - ***BSW1 <.....>*** *Value between 0 to +255*
    - ***BSW2 <.....>*** *Value between 0 to +255*
    - ***BSW3 <.....>*** *Value between 0 to +255*
    - ***Low-Mid – Low Byte <.....>***
    - ***Low-Mid – High Byte <.....>***
    - ***Mid-High – Low Byte <.....>***
    - ***Mid-High – High Byte <.....>***

S Band TOP <.....>
VIF TOP <.....> *Value between 0 to +15*
VIF TOP SECAM <.....> *Value between 0 to +15*
VIF TOP DK<.....> *Value between 0 to +15*
Synch Threshold<.....> *Value between 0 to +40*

17.4 Options

Options-1
- ***Power Up***
  - ***Standby***
  - ***Last state***
- ***TV Open Mode***
  - ***Source***
  - ***1st TV***
  - ***Last Tv***
- ***First APS <.....>***
  If "Yes" selected, first time TV opens by asking APS.
- ***APS Volume <.....>*** *Value between 0 to +63*
- ***Burn In Mode <.....>***
  If "Yes" selected, TV opens with Burn-In mode. This mode is used in manufacturing.
- ***APS Test***

Autostore <.....>

If “Yes” selected, Channel is automatically stored.

Unicode Enabled <.....>

If “Yes” selected,Unicode characters can be read in the USB Files.

Options-2

Source List menu <.....>

If “Yes” selected, Sorce List Menu appears on the screen when press “source” button.

RC Select <.....>

RC Group 1
RC Group 2
RC Group 3
RC Group 4
RC Group 5
RC Group 6

Double Digit Key <.....>

If “Yes” selected, Double Digit Button on RC activates.

Protection <.....>

If “Yes” selected,short circuit protection activates.

Led Type <.....>

1 Led 1 Color
1 Led 2 Color
2 Led 2 Color
1 Led 3 Color
2 Led 3 Color

200 Programme <.....>

If “Yes” selected, totaly 200 programmes can be used.

TouchPad <.....>

If “Yes” selected, TouchPad can be used.

Teletext Options

TXT Darkness <.....> *Value between 0 to +63*

TXT Type <.....>

Fasttext&Toptext
No
Default
Fastext
Toptext

TXT Language <.....>

Menu
West
East
Cyrillic
Turk/Gre
Arabic
Persian
Auto

No Txt Warning <.....>

If "Yes" selected, "No Txt Transmission" warning appears on the screen when pressing txt button from RC.

Txt Subtitle <.....>

If "Yes" selected, Teletext subtitles can be seen.

Optional Features

Default Zoom <.....>

Menu
16:9
4:3
Panaromic
14:9 Zoom

Menu Timeout <.....>

Menu
15 Sec
30 Sec
60 Sec
No Time

Backlight <.....>

*If "Yes" selected, **"Backlight"** feature is active.*

100 Step Slider <.....>

If "Yes" selected, 64 step sliders will become 100 step sliders.

Analog USB Enabled <.....>

*If "Yes" selected, **"Analog USB"** option is active.*

Menu Double Size <.....>

If "Yes" selected, menu sizes increases.

CEC Enable <.....>

*If "Yes" selected, **"CEC"** feature is active.*

Digital USB Hotplug <.....>

*If "Yes" selected, **"Digital USB Hotplug"** feature is active.*

PIP Options

Pip <.....>

AV PIP
No PIP
PC PIP

Hotel Options <.....>

Hotel TV <.....>

*If "Yes" selected, **"Hotel TV"** feature is active.*

IR Smartloader <.....>

*If "Yes" selected, **"IR Smartloader"** feature is active.*

17.5 External Source Settings

TV <.....>
DTV <.....>
Ext 2 <.....>
Ext 2 S <.....>
FAV <.....>
BAV <.....>

S-Video <.....>
HDMI 1 <.....>
HDMI 2 <.....>
HDMI 3 <.....>
HDMI 4 <.....>
YPbPr <.....>
PC <.....>

17.6 Preset

User Ad.j
ADC Adj.
Service Adj.
All Adj.
Init Factory Channels.

17.7 NVM Edit

NVM-edit addr. (hex)
NVM-edit data (hex)
NVM-data dec

17.8 Programming

HDMI DDC Update Mode <.....>
HDCP Key Update Mode <.....>
Software Bypass <.....>
If "On" selected, speaker effects are bypassed.

LVDS Clock Step <.....> *Value between 0 to +255*
Memory Clock Step <.....> *Value between 0 to +255*
DTV Download <.....>
If "On" selected, DTV software can be updated from SCART.
DSUB9 Download <.....>
If "On" selected, DTV software can be updated from DSUB9.

17.9 Diagnostic

Eeprom I2C
Tuner I2C
IF I2C
HDMI I2C

17.10 Product Info

18 SOFTWARE UPDATE DESCRIPTION

16.1 17MB37 Analog Part Software Update With Bootloader Procedure

1.1 The File Types Used By The Bootloader

All file types that used by the bootloader software are listed below:

1. The Binary File : It has ".bin" extension and it is the tv application. Its size is 1920 Kb.

2. The Config Binary File : It has ".cin extension and it is the config of the tv application. Its size may be 64 Kb or a few times 64 Kb.

3. The Test Script File : It has ".txt" extension and it is the test script that is parsed and executed by the bootloader. It don't have to be any times of 64 Kb.

4. The Test Binary File : It has ".tin" extension and it is used and written by the test groups. It is run to understand the problem part of the hardware.

Alltough a file that is used by the bootloader can be had any one of these extensions, its name has to be "VESTEL_S" and it has to be located in the root directory of the usb device.

1.2 Usage of The Bootloader

1. The starting to pass through : The chassis is only powered up.
2. The starting to download something : When chassis is powered up the menu key has to be pushed.Before the chassis is powered up and if any usb device is plugged to the usb port, the programme is downloaded from usb firstly.

Any usb device is plugged to usb port , user must open hyperterminal in the pc and connect pc to chassis via Mstar debug tool and any one of scart,dsub9 or I2c connectors. Serial connection settings are listed below:

- Bit per second: 115200
- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None

In this case the bootloader sofware puts "C" character to uart. After repeating "C" characters are seen in the hyperterminal user can send any file to chassis by selecting Transfer -> Send File menu item and choosing "**1K Xmodem**" from protocol section.

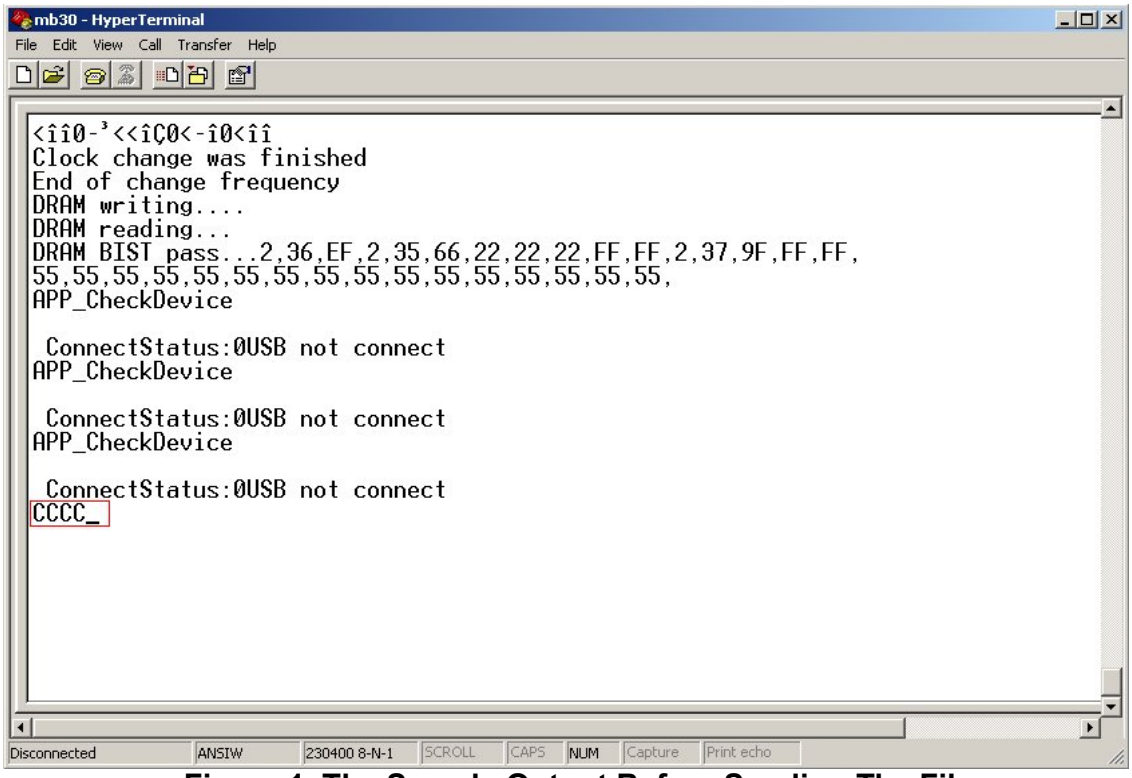


Figure 1. The Sample Output Before Sending The File

2. EEProm update

To Update eeprom content via uart scart,dsub9 or i2c with Mstar tool can used.
Serial connection settings are listed below:

- Bit per second: 9600
- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None

Programming menu item is choosed in the service menu and switch “HDCP Key Update Mode” from off to on.

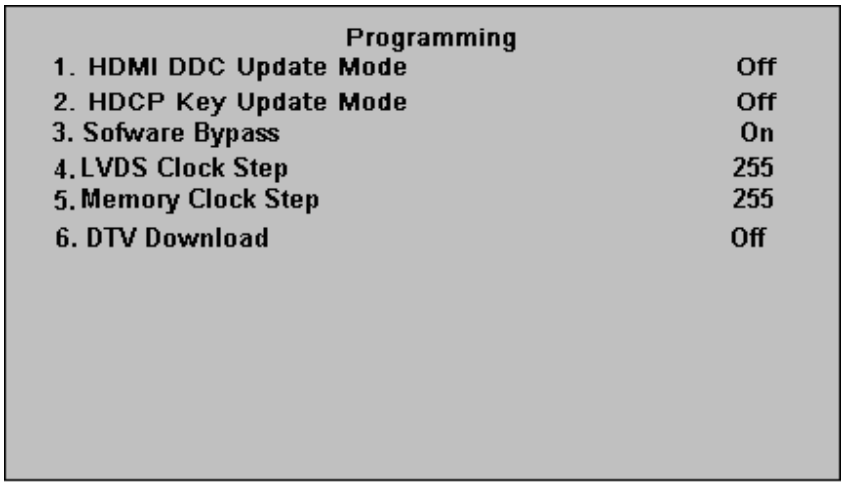


Figure 2. The Programming Service Menu

After then you must see Xmodem menu in the hyperterminal.To download hdcp key press k or to download eeprom content press w.

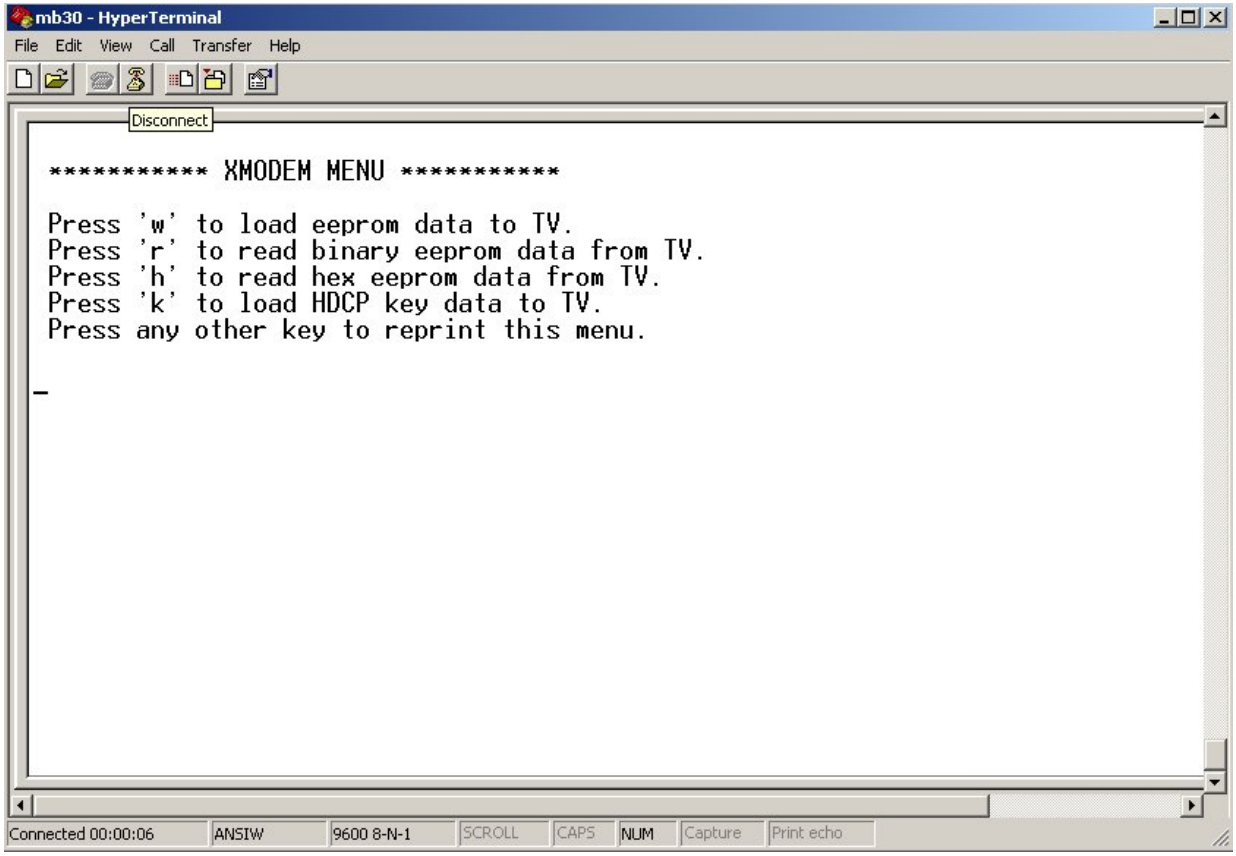


Figure 3. Xmodem Menu

If the repeated “C” characters are seen you can transfer file content via select Transfer->Send File and choose “**Xmodem”** protocol and click the “Send” button.

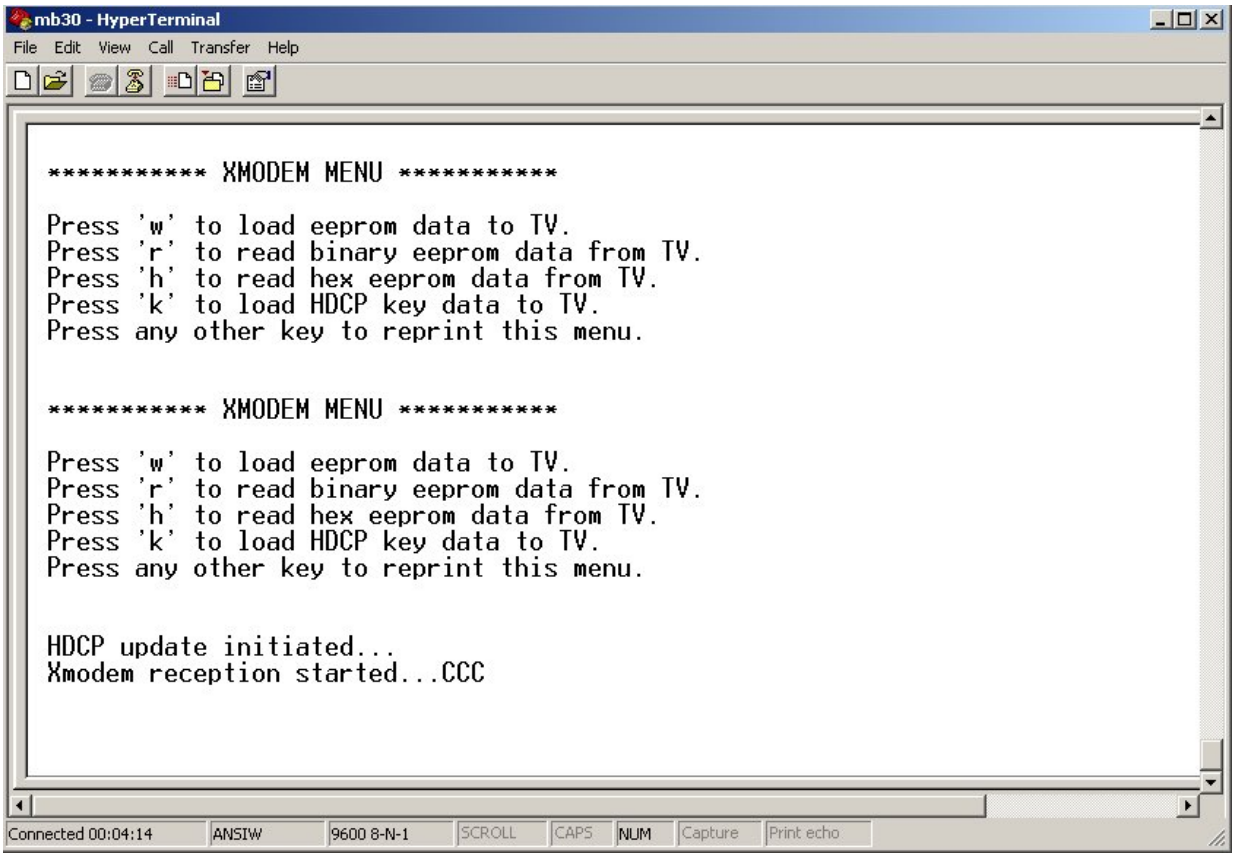


Figure 4. The Starting To Send

16.2 17MB37 HDCP key upload procedure.

1) Turn on TV set.
2) Open a COM connection using fallowing parameters and select ISP COM Port No

Baud Rate: 9600 bps
Data Bits: 8
Stop Bits: 1
Parity: None
Flow Control: None

3) Enter service menu by pressing “4” “7” “2” 5” consecutively while main menu is open
4) Select “9. Programming”
5) Select “HDMI HDCP Update Mode” yes.
6) On Hyper Terminal Window press “k”
7) Click on send file under Transfer Tab.
8) Select Xmodem and choose the HDCP key to be uploaded.
9) Press send button
10) Restart TV set

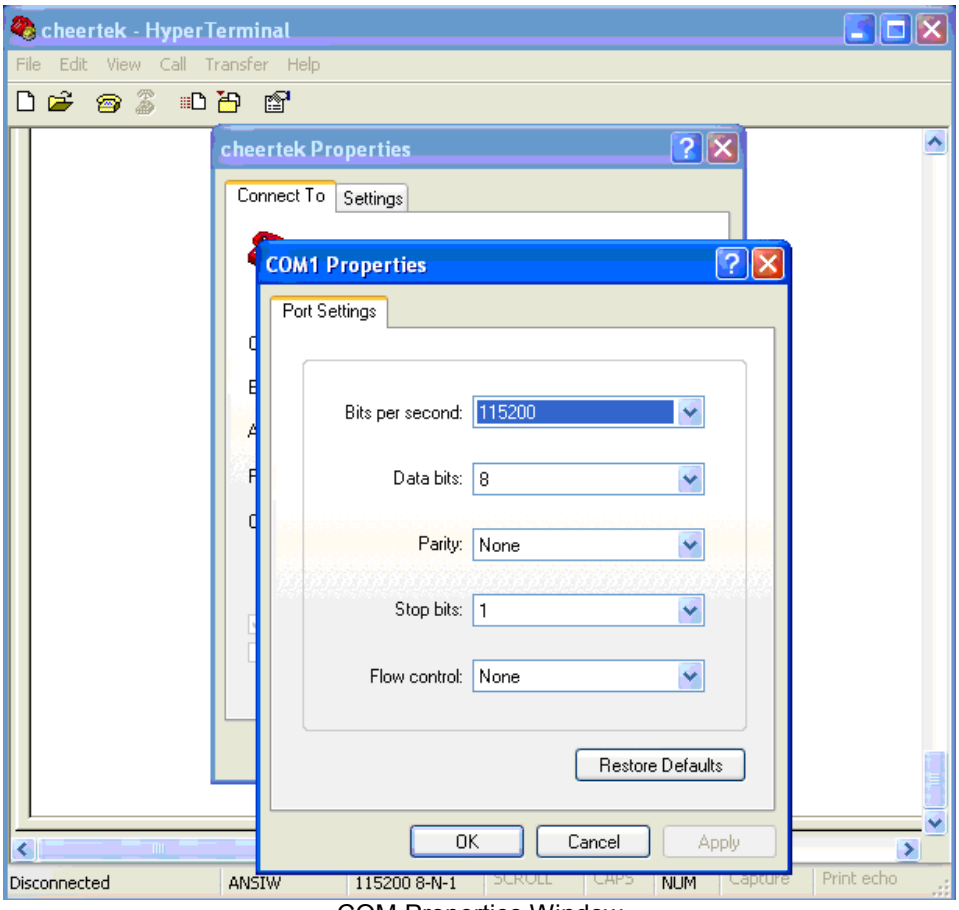
16.3 17MB37 Digital Software Update From SCART

Adjusting DTV Download Mode:

1. Power on the TV.
2. Exit the Stby Mode.
3. Enter the “Tv Menu”.
4. Enter “4725” for jumping to “Service Settings”.
5. Select “8. Programming” step.
6. Change “6. DTV Download” to “On”.
7. Switch to the Stby mode.

Adjusting HyperTerminal:

1. Connect the “MB37 SCART Interface” to SCART1 (bottom SCART plug).
2. Also connect the “MB37 SCART Interface” to PC.
3. Open “HyperTerminal”.
4. Determine the “COM” settings listed and showed below.
   - Bit per second: 115200
   - Data bits: 8
   - Parity: None
   - Stop bits: 1
   - Flow control: None

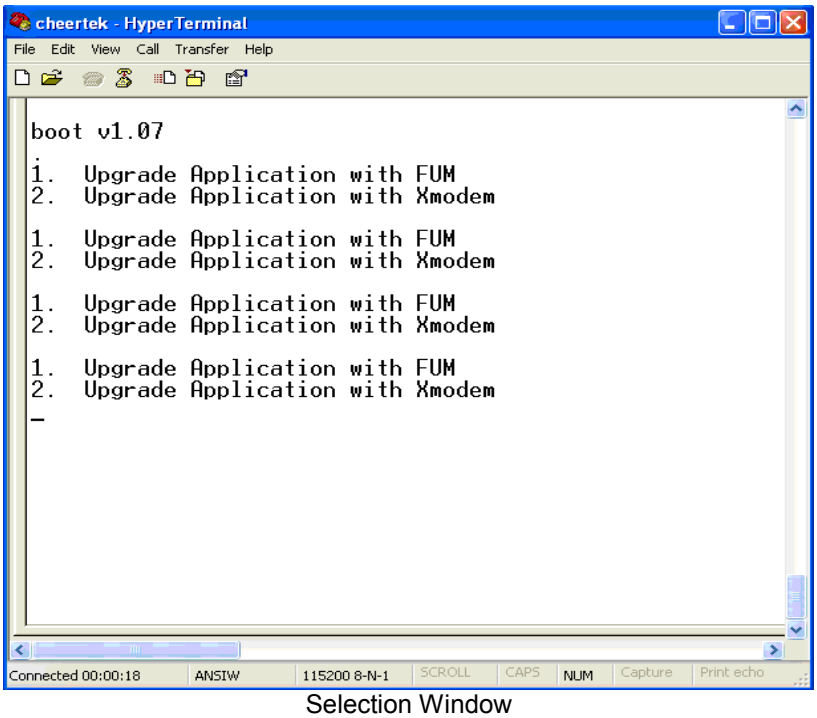


COM Properties Window

6. Click “OK”.

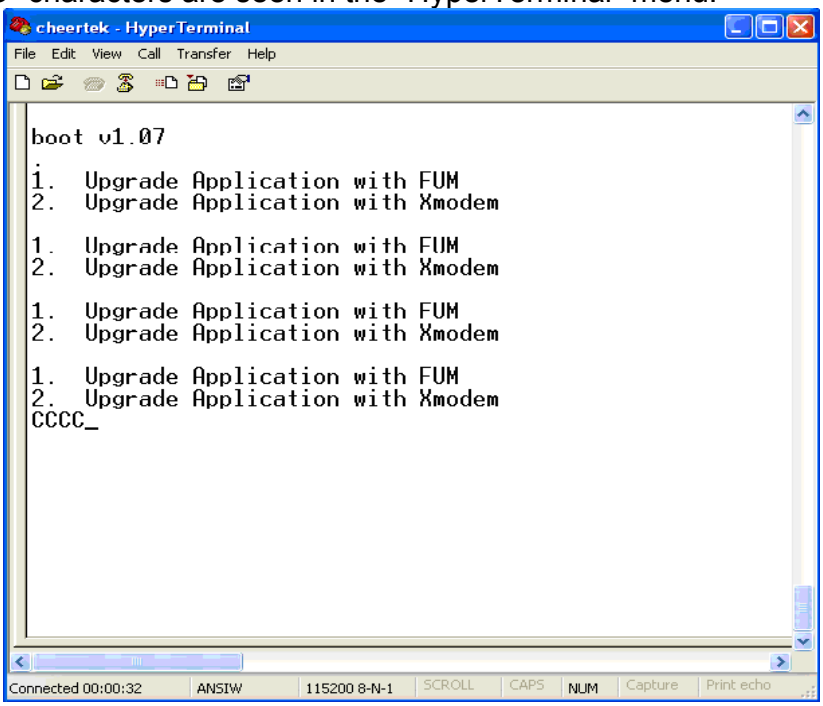
Software Updating Procedure

1. In the HyperTerminal Menu, click the “Connect” button.
2. Exit the Stby Mode.
3. The “Space” button on the keyboard must be pressed, when the following window can be seen.



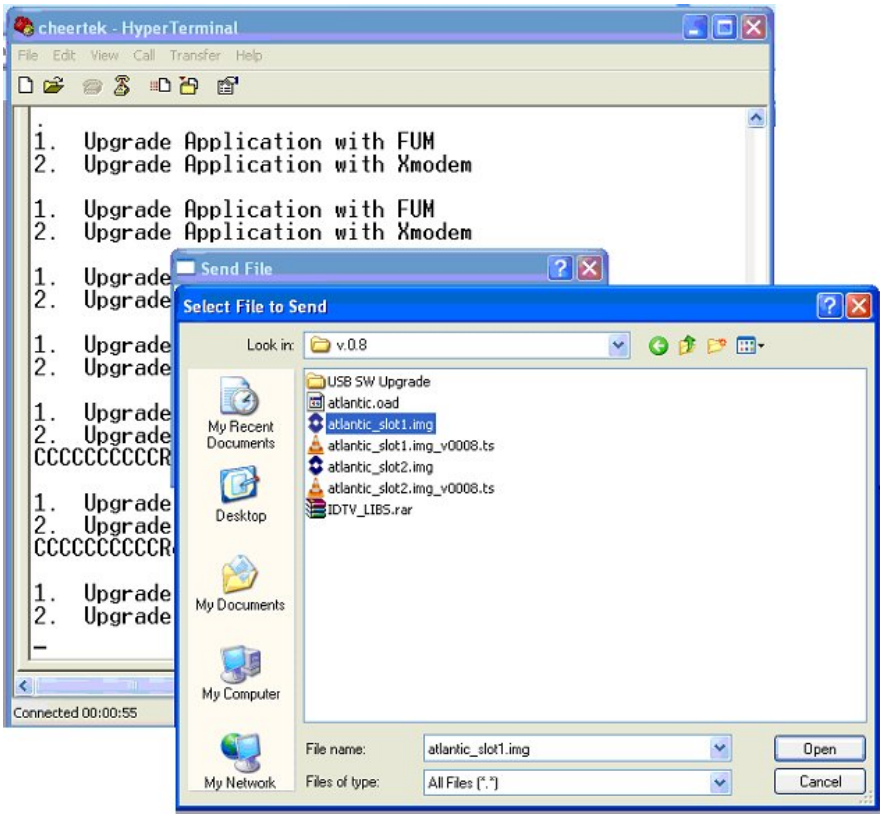
Selection Window

4. Press the “2” button on the keyboard for choosing “2. Upgrade Application with Xmodem”.
5. Repeating “C” characters are seen in the “HyperTerminal” menu.

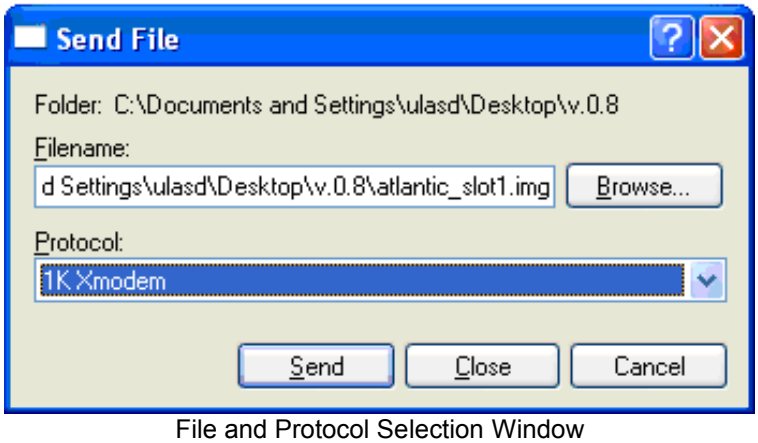


The Sample Output Before Sending The File

6. Click the “Send” button on the HyperTerminal
7. Select the “Filename **xxxx**_slot1.img” using “Browse”.
8. Choose the “1K Xmodem” from “Protocol” option.

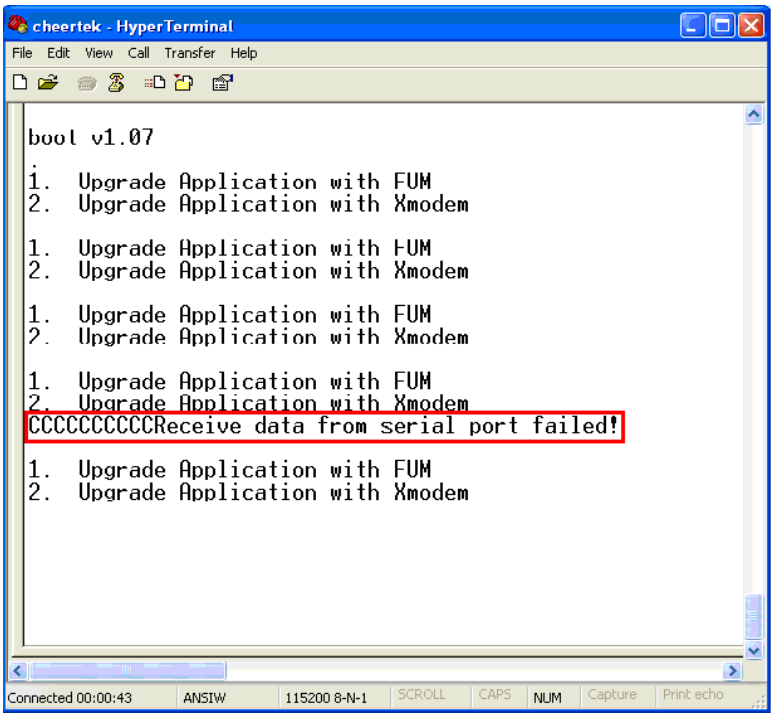


Selection of File



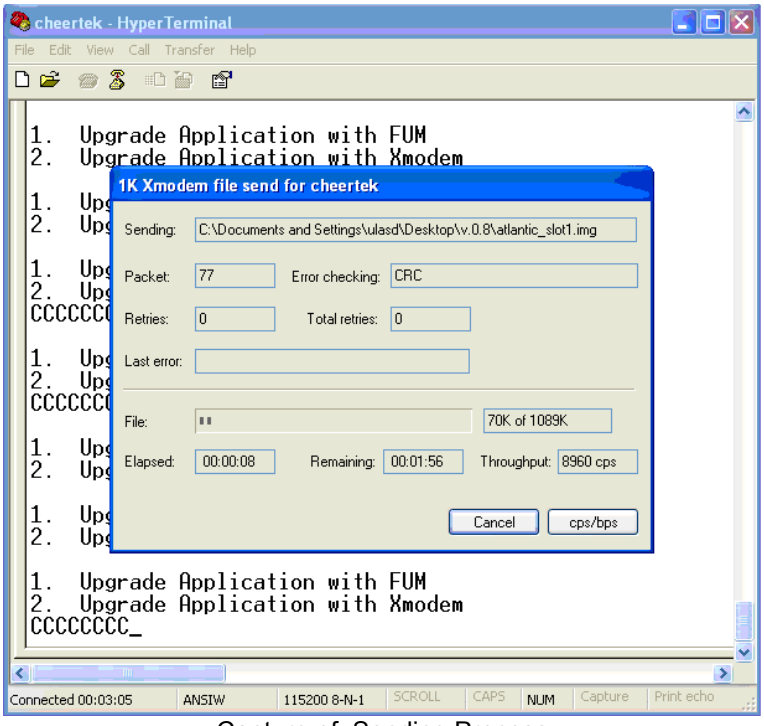
File and Protocol Selection Window

Note: In the Software updating Procedure section, when the first “C” character is seen, the filename selection process must be finished before 10 seconds. If the process can not be finished, the file sending operation will be cancelled. The following figure shows this situation.



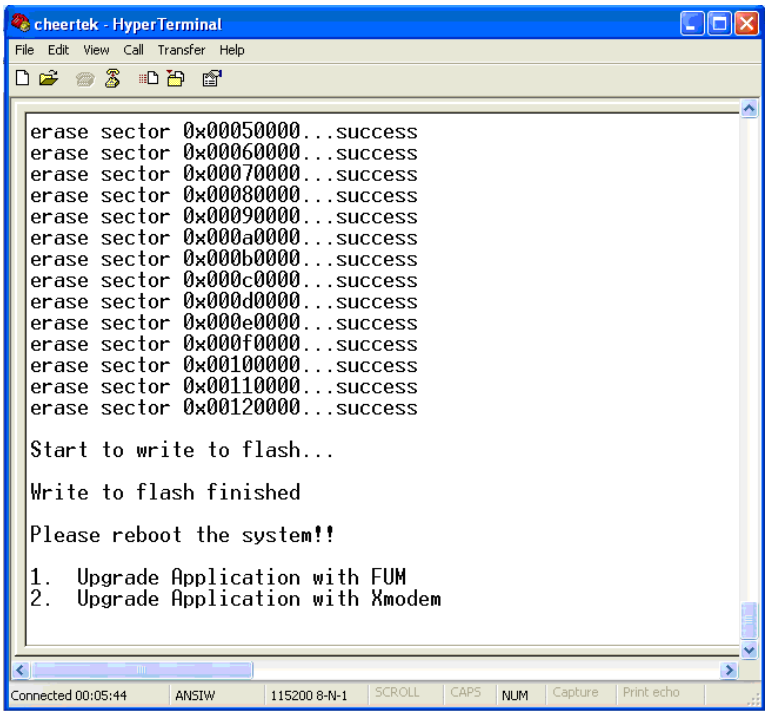
Capture of Receving Data Failing

9. When sending the file the following window must be seen.



Capture of Sending Process

10. After the sending process the following HyperTerminal window must be seen.

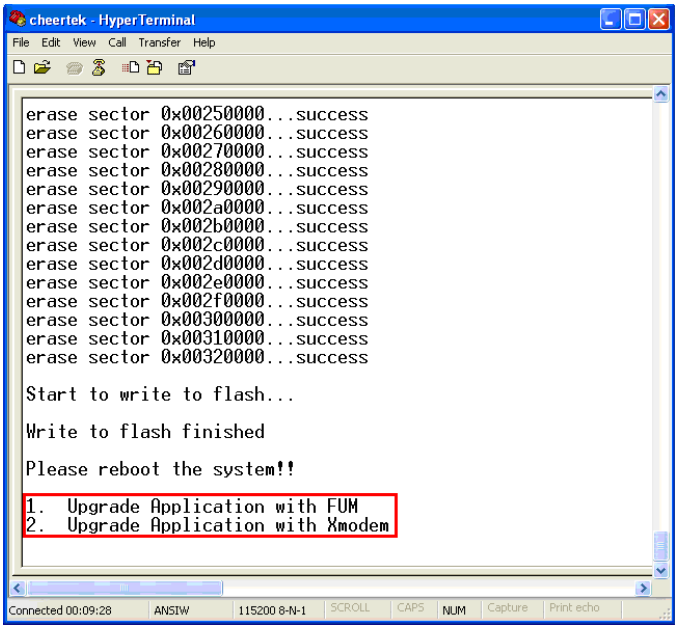


Capture of End of The Sending Process

11. For sending second program file, the Software Updating Procedure must be repeated from the step **X**. Select the “Filename **xxxx**_slot2.img” using “Browse”.
12. After sending the second program file, the Software Updating Procedure will be succesful.

Note: After the File Sending Process,

1. Upgrade Application with FUM
2. Upgrade Application with Xmodem, options must be seen.



End of The Sending Process

Checking Of The New Software
1. Turn off and on the TV.
2. Enter the “Setup” submenu in the “DTV Menu”.
3. Choose the “Configuration” option.
4. For controlling new software, check the “Receiver Upgrade” option.

16.4 17MB37 Digital Software Update From USB

Software upgrade is possible via USB disk by folowing the steps below.

1. Copy the bin file, including higher version than the software loaded in flash, into the USB flash memory root directory. This file should be named up.bin.
2. Insert the USB disk.
3. Digital module performs version and CRC check. If version and CRC check is successful, then a message prompt appears to notify user about new version. If the user confirms loading of new version, upgrade.bin file is written into flash unused slot.
4. Digital module disables the previous software in the flash and then a system reset is performed.
5. After the reset, digital module starts with new software.

Revert operation:

With revert operation, it is possible to *downgrade* the software.
Revert operation is very similar to upgrade process. In the revert operation, file name should be f_up.bin. Also user confirmation is not asked.

1. Copy the bin file into the USB flash memory root directory. This file should be named force_upgrade.bin.
2. Insert the USB disk.
3. A lower version than the software in flash can be loaded with revert operation. Digital module performs only CRC check. If CRC check is successful, then force_upgrade.bin file is written into flash unused slot.
4. Digital module disables the previous software in the flash.
5. A message prompt is displayed to notify user about end of revert process.
6. Power off/on is required to start digital module with the new software.

For controlling new software, check the “Receiver Upgrade” option.

19 BLOCK DIAGRAMS

19.1 General Block Diagram

I2C_5V
I2C_TUN_DVB
RF_AGC_DVB
74HCT4053 I2C & AGC SWITCH
RF_AGC_A
I2C
RF AGC
DIGITAL IF
THOMSON DTT75430 LG TDTC-GXX1D
ANALOG IF
DVB-T COFDM DEMOD. STV0362
DVB-C QAM DEMOD. STV0297
TS_T
TS_C
FSA3157 IF AGC SWITCH
IF AGC
IF AGC_C
IF AGC_T
This Block does not exist, unless PCB has enough space
TS_CI
RJ45
ETHERNET PHY STE101P
MPEG4 DECODER STi7101
2xFLASH NOR 64Mbit (common) NAND 2Gbit (w/ethernet)
4xDDR1 16Mx16
BUFFERS 74LCX244
CI_BUFFERS
TS_CI
USB HUB USB2503
YPbPr
SPDIF
UART
14.3181MHz XTAL
RESET IC MAX809LTR
EEPROM 24C32
1MB Serial Flash
2MB SD RAM
SCL/SDA2
LVDS CONNECTOR
PANEL SUPPLY
PANEL VCC SW
PANEL_VCC
StBy M TV/AV +P -P +V -V
USB
USB
SAW K9656M
SAW K3958M
I2C LEVEL SHIFTER CIRCUIT
SCL/SDA
I2C_5V
I2C
PANEL_VCC_ON/OFF
KEYBOARD
VIF_TUNER
SIF_TUNER
I/O PORTS
I/O PORTS
LED1
LED2
DDC_WP
PANEL_VCC_ON/OFF
POWER ON/OFF
SCART1 PIN8
MPEG DECODER IRQ
PROTECTION
NVM_WP
MST6Wx7
USB
SCART
SC1 CVBS
SC1 RGB/FB
SC1 AUD_IN
SC1_CVBS_OUT
SC1_AUD_OUT
+3V3_STBY
+1V2_STBY
+2V6
+3V3
+12V
AUDIO AMP. PT2333 or MP1720 2 x 2.5W
Main Speaker 4R
MAIN SPEAKER OUT L/R
HP OUT L/R
+5V
HP AMPLIFIER TDA1308T
DETACHED HP MUTE
POP NOISE CIRCUIT
ON/OFF
TRANSISTOR SWITCH
I2C2/UART
HDMI1
HDMI2
DDC
TMDS DATA/CLK
EDID E2PROM 24C02
EDID E2PROM 24C02
HDMI_1
HDMI1 TMDS DATA/CLOCK 2
HDMI_2
Y/C
SVHS
CVBS
AUDIO L/R
FAV_Video/Audio
YPbPr
VGA/YPbPr AUDIO L/R
LINE OUT L/R
LINE OUT
DDC
PI5V330 RGB Switch
IDTV/YPbPr_SW
IDTV_YPbPr/SOY
YPbPr
VGA
DVD Y/C_IN
DVD AUDIO_IN
DVD Connector
DVD_SENSE
DVD Power Connector
+12V
IR
IR ON/OFF
BACKLIGHT_ON/OFF
BACKLIGHT_DIMMING
POWER_ON/OFF
+24V
+12V
+5V_STBY
+5V
+3V3_STBY
+3V3
POWER MODULE

4 Layer PCB

VESTEL ELECTRONICS R&D GROUP
17MB37 BLOCK DIAGRAM
DATE:03.03.2009
DRAWN BY: SADIK ŞEHİT

LG

TU102 TDTC-G101D

AIF 12 ANALOG_IF
DIF1 11 TUNER_PIN11
DIF2 10 TUNER_PIN10
IF_AGC 9 IF_AGC_DVB_IN
AS 8 ADDRESS_SEL_TUNER
NC 7
B2 6 5V_TUN
SDA 5 SDA_TUNER
SCL 4 SCL_TUNER
RF_AGC 3 RF_AGC
B1 2 33V_TUNER
ANT_PWR 1 ACT_ANT

Samsung/Thomson

TU101 DTOS403LH172A

IFOUT- 11
IFOUT+ 10 TUNER_PIN10
VT 9 33V_TUNER
IF_AGC 8 IF_AGC_DVB_IN
+5V 7 5V_TUN
AIF_OUT 6 S308 ANALOG_IF
SDA 5 SDA_TUNER
SCL 4 SCL_TUNER
SAS 3 ADDRESS_SEL_TUNER S104
RF_AGC 2 RF_AGC
BA 1 ACT_ANT

TUNER_PIN11 L116 1u C626 47p 50V
TUNER_PIN11 C913 1n 50V DIGITAL_IF-
C1029 2p2 50V
TUNER_PIN10 C914 1n 50V DIGITAL_IF+

ACT_ANT TP151

ACTIVE ANTENNA

5V_TUN R482 4R7 2R1 TH101
OVER_CUR_DETECT R502 10k 330R F234
R501 10k
5V_TUN
R622 1k
Q102 FDN336P
BC848B Q115
R503 10k ANT_CTRL
C359 10u 10V
R504 10k

D121 1N4148
RF_AGC_A R111 12k T_AGC
C448 47u 16V N.C.
IF_AGC_DVB_IN R505 10k IF_AGC_DVB
10V 100n C136

This part must be placed near the tuner

SCL_TUNER R126 47R SCL_TUN
C586 47p 50V
SDA_TUNER R127 47R SDA_TUN
C587 47p 50V

TUNER SUPPLY OPSION

8V_VCC F116 330R
C600 47u 16V
U123 LM1117 IN OUT GND VOUT
R408 1k 330R
C360 10u 10V
C134 100n 10V
C1158 220u 6V3
5V_TUN
R460 330R S105
Near Tuner supply pin

!!!En az 1.8 cm2 altta ve üstte soðutma alaný býrakýlmalý. 1K

AGC AND I2C SWITCH PART

33V_TUNER C532 1u 50V
R624 1k
F159 330R 5V_TUN
5V_VCC
C128 100n 10V
U115 74HCT4053
SCL_TUN_DVB 1 2Y1
SCL 2 2Y0
RF_AGC_DVB 3 3Y1
3Z 4
RF_AGC_A 5 3Y0
E 6
VEE 7
GND 8
VCC 16
2Z 15
1Z 14
1Y1 13
1Y0 12
S1 11
S2 10
S3 9
SCL_TUN
SDA_TUN
SDA_TUN_DVB
SDA
R254 4k7 5V_VCC
RF_AGC
10V 100n C137 NEAR THE TUNER
Q116 BC848B
R595 22K IDTV_SW

OPTIONAL COIL

5V_TUN R1300 220R C520 47u 16V
R38 220R
R252 4k7
C135 100n 10V
R483 1k2
1u L101 1u L114
680R R735
R125 47R
ANALOG_IF L111 1u C545 10n 16V R680 56R
Q144 BF799
R623 1k
R384 10R

5V_TUN R473 6k8 R231 3k3
C546 10n 16V
BA782 D145
Z101 IN1 OUT1 K9656M IN2 OUT2 GND
SIFP
SIFM
R474 6k8
5V_TUN
22k R594
SIF_CTL
R209 100k
Q140 BSN20
R210 100K N.C.
C547 10n 16V
Z102 IN1 OUT1 K3958M IN2 OUT2 GND
L104 2u2 N.C.
VIFM
VIFP

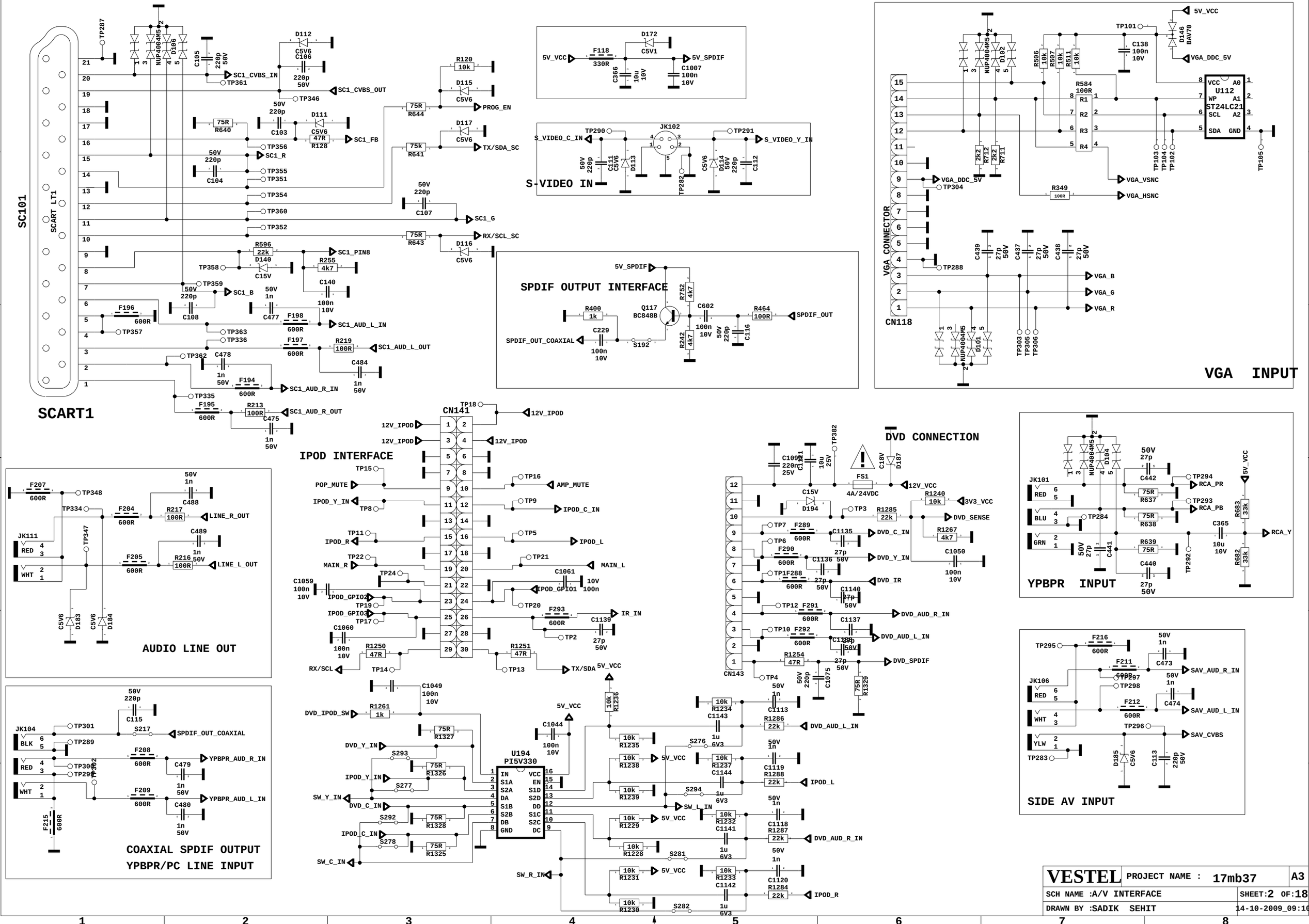
WARNING!!! Saw filter outputs must be close the chip

V-1 e gecerken yapilan updateler

Video SAW filitre cikislari caprazlandý

C467 10u 10V
C132 100n 10V
C611 220u 6V3
C636 220n 10V
C597 220p 50V
C620 100p 50V
WARNING!!! This part must be close to chip
3V3_STBY F187 330R
C363 10u 10V
C131 100n 10V
U138 MST6WB7GQ-3
AVDD_MPLL 62
VR27 63 4
VR12 64
AVDD_RXS 65
GND_RXS 66
SIFP 67
SIFM 68
VIFM 69
VIFP 70
GND_RXV 71
AVDD_RXV 72
TAGC 73
3V3_VCC F184 330R
C364 10u 10V
C130 100n 10V
C361 10u 10V
C129 100n 10V
3V3_VCC F185 330R
5V_TUN F186 330R
C510 100n 10V
4k7 R253
T_AGC
WARNING!!! This part must be close to chip

VESTEL	PROJECT NAME : 17mb37	A3
SCH NAME :ANALOG IF	SHEET:1 OF:18	
DRAWN BY :SADIK SEHIT	14-10-2009_09:09	


SCART1
SC101
SCART LT1
SC1_CVBS_IN
SC1_CVBS_OUT
SC1_FB
SC1_R
SC1_G
SC1_B
SC1_PIN8
SC1_AUD_L_IN
SC1_AUD_L_OUT
SC1_AUD_R_IN
SC1_AUD_R_OUT
PROG_EN
TX/SDA_SC
RX/SCL_SC
S-VIDEO IN
S_VIDEO_C_IN
S_VIDEO_Y_IN
SPDIF OUTPUT INTERFACE
SPDIF_OUT_COAXIAL
SPDIF_OUT
IPOD INTERFACE
POP_MUTE
AMP_MUTE
IPOD_Y_IN
IPOD_C_IN
IPOD_R
IPOD_L
MAIN_R
MAIN_L
IPOD_GPIO2
IPOD_GPIO1
IPOD_GPIO3
IR_IN
RX/SCL
TX/SDA
12V_IPOD
DVD CONNECTION
DVD_SENSE
DVD_C_IN
DVD_Y_IN
DVD_IR
DVD_AUD_R_IN
DVD_AUD_L_IN
DVD_SPDIF
VGA CONNECTOR
VGA_DDC_5V
VGA_VSNC
VGA_HSNC
VGA_B
VGA_G
VGA_R
VGA INPUT
YPBPR INPUT
RCA_PR
RCA_PB
RCA_Y
SIDE AV INPUT
SAV_AUD_R_IN
SAV_AUD_L_IN
SAV_CVBS
AUDIO LINE OUT
LINE_R_OUT
LINE_L_OUT
COAXIAL SPDIF OUTPUT
YPBPR/PC LINE INPUT
YPBPR_AUD_R_IN
YPBPR_AUD_L_IN
U194
PI5V330
CN141
CN118
CN143
U112
ST24LC21
JK102
JK101
JK104
JK106
JK111
VESTEL
PROJECT NAME : 17mb37
A3
SCH NAME :A/V INTERFACE
SHEET:2 OF:18
DRAWN BY :SADIK SEHIT
14-10-2009_09:10

VIDEO TERMINATIONS AND DIFFERENTIAL TRACING
Place 75R termination resistors
close to Paulo reference GNDs

SW_C_IN — R651 75R — R143 47R — C432 16V 47n — C0
SW_Y_IN — R650 75R — R142 47R — C434 47n 16V — Y0
S_VIDEO_C_IN — R653 75R — R145 47R — C423 16V 47n — C1
S_VIDEO_Y_IN — R652 75R — R144 47R — C422 47n 16V — Y1
SC1_CVBS_IN — R654 75R — R146 47R — C424 47n 16V — CVBS1
R773 470R — C612 1n — SOGIN0
SAV_CVBS — R649 75R — R141 47R — C433 50V 47n 16V — CVBS2
DVB_CVBS — R664 75R — R140 47R — C435 47n 16V — CVBS3
SC1_B — R665 75R — R137 47R — C421 47n 16V — BIN0P
SC1_G — R667 75R — R138 47R — C418 47n 16V — GIN0P
SC1_R — R666 75R — R139 47R — C417 47n 16V — RIN0P
SW_PB — R656 75R — R149 47R — C428 47n 16V — BIN2P
SW_Y — R648 47R — C426 47n 16V — GIN2P
R657 75R — R403 470R — C490 1n 50V — SOGIN2
SW_PR — R655 75R — R147 47R — C427 47n 16V — RIN2P
VGA_B — R659 75R — R829 47R — C429 47n 16V — BIN1P
VGA_G — R831 47R — C431 47n 16V — GIN1P
R658 75R — R404 470R — C491 1n 50V — SOGIN1
VGA_R — R660 75R — R830 47R — C430 47n 16V — RIN1P

U138
MST6WB7GQ-3

VGA_HSNC	17	HSYNC1	AVDD_AU_1	74	AVDD_AU (C148 100n 10V, 10V 10u)
VGA_VSNC	18	VSYNC1	GND5	75	
C152 100n 10V	19	VCLAMP	AUVRM	76	(10V 10u C369)
C151 100n 10V	20	REFP	AUVRP	77	(C368)
C150 100n 10V	21	REFM	AUVAG	78	(C659 100n 16V)
BIN1P	22	BIN1P	AVDD_AU_2	79	AVDD_AU
SOGIN1	23	SOGIN1	LINE_IN_0L	80	LINE_IN_0L
GIN1P	24	GIN1P	LINE_IN_0R	81	LINE_IN_0R
RIN1P	25	RIN1P	LINE_IN_1L	82	LINE_IN_1L
R133 47R — C420 47n 16V	26	BIN0M	LINE_IN_1R	83	LINE_IN_1R
BIN0P	27	BIN0P	AUCOM	84	C149 — S106
R134 47R — C419 47n 16V	28	GIN0M	LINE_IN_2L	85	100n 10V — LINE_IN_2L
GIN0P	29	GIN0P	LINE_IN_2R	86	LINE_IN_2R
SOGIN0	30	SOGIN0	LINE_IN_3L	87	LINE_IN_3L
RIN0P	31	RIN0P	LINE_IN_3R	88	LINE_IN_3R
AVDD_33	32	AVDD_33_3	LINE_IN_MONO	89	R686 33k
C143 100n 10V	33	GND3	LINE_OUT_3L	90	DSP_CH2_L
	34	HSYNC0	LINE_OUT_3R	91	DSP_CH2_R
SC1_FB	35	VSYNC0	LINE_OUT_2L	92	DSP_CH4_L
R687 33k	36	VSYNC2	LINE_OUT_2R	93	DSP_CH4_R
BIN2P	37	BIN2P	LINE_OUT_1L	94	DSP_CH1_L
SOGIN2	38	SOGIN2	LINE_OUT_1R	95	DSP_CH1_R
GIN2P	39	GIN2P	LINE_OUT_0L	96	DSP_CH3_L
RIN2P	40	RIN2P	LINE_OUT_0R	97	DSP_CH3_R
C1	41	C1			
Y1	42	Y1			
C0	43	C0			
Y0	44	Y0			
CVBS3	45	CVBS3			
CVBS2	46	CVBS2			
CVBS1	47	CVBS1			
C425 47n	48	VCOM1			
R859 10k	49	CVBS0			
C416 47n	50	VCOM0			
AVDD_33	51	AVDD_33_4			
C144 100n 10V	52	CVBSOUT1			
	53	CVBSOUT0			
	54	GND4			

CVBS0_OUT — R351 100R

AVDD_AU DECOUPLING CAPACITORS
Pin79: AVDD_AU — C142 100n 10V
Pin74: C145 100n 10V — F120 330R — 3V3_VCC

SCART VIDEO OUTPUT AMPLIFIERS

5V_VCC — F119 330R
C666 1u 16V
R402 470R, R674 39k
Q146 BC858B
Q119 BC848B — C378 10u 10V — CVBS0_OUT
SC1_CVBS_OUT — R646 75R — R620 300R
R777 75R, 100R R221, R467 15k
GAIN_SW1 — R753 4k7 — Q154 2N7002

AUDIO INPUT VOLTAGE DIVISION AND DC BLOCK
Place close to Paulo

LINE_IN_0L — C656 100n 16V — R513 10k — R607 22k — SC1_AUD_L_IN
LINE_IN_0R — C655 100n 16V — R514 10k — C493 1n 50V — R606 22k — SC1_AUD_R_IN
LINE_IN_1L — C645 100n 16V — R515 10k — C492 1n 50V — R605 22k — SW_L_IN
LINE_IN_1R — C644 100n 16V — R516 10k — C495 1n 50V — R603 22k — SW_R_IN
LINE_IN_2L — C642 100n 16V — R517 10k — C494 1n 50V — R601 22k — YPBPR_AUD_L_IN
LINE_IN_2R — C643 100n 16V — R518 10k — C497 1n 50V — R600 22k — YPBPR_AUD_R_IN
LINE_IN_3L — C660 100n 16V — R519 10k — C496 1n 50V — R599 22k — SAV_AUD_L_IN
LINE_IN_3R — C661 100n 16V — R520 10k — C498 1n 50V — R598 22k — SAV_AUD_R_IN
C499 1n 50V

AUDIO PREAMPLIFIERS
Place close to Paulo

SC1_AUD_R_OUT — 10V 10u C375 — C121 220p 50V — R692 33k — R678 82k
SC_1_R — C649 100n 16V — R739 20k
C631 100n 16V — F217 600R — 8V_VCC
R691 33k — 10V 10u C374 — SC1_AUD_L_OUT
C120 220p 50V — R677 82k
R738 20k — C650 100n 16V — SC1_L
U118 TL062 (OUT1, VDD, IN1-, OUT2, IN1+, IN2-, V+, VSS, IN2+, V+)

R689 33k — R690 33k
LINE_R_OUT — 10V 10u C372 — R155 47R
8V_VCC — F219 600R — C630 100n 16V
50V 220p — C119 R676 82k
POP_MUTE — R522 10k — Q121 BC848B — R751 3k3
LINE_OUT_R — C662 100n 16V — R737 20k
R153 47R — 10V 10u C371 — LINE_L_OUT
50V 220p — C118 R675 82k
Q120 BC848B — R521 10k — POP_MUTE; 3k3 R750
R736 20k — C663 100n 16V — LINE_OUT_L
U117 TL062 (OUT1, VDD, IN1-, OUT2, IN1+, IN2-, V+, VSS, IN2+, V+)

V+ — C646 100n 16V — C586 10u 10V — 33k R684 — 33k R685 — 8V_VCC

DVB/YPBPR SWITCH

C443 27p 50V — DVB_PR — R661 75R
DVB/YPBPR_SW — R627 1k
RCA_PR
SW_PR
DVB_Y — C444 27p 50V — R662 75R
RCA_Y
SW_Y
U129 PI5V330 (IN, S1A, S2A, DA, S1B, S2B, DB, GND, VCC, EN, S1D, S2D, DD, S1C, S2C, DC)
10V 100n — C147 10u — C1006 — 10V
D167 C5V1 — F151 330R — 5V_VCC — C445 27p — DVB_PB — R663 75R
RCA_PB
SW_PB

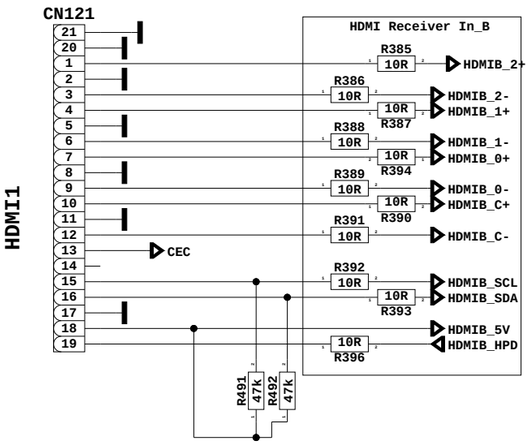
DSP_CH2_L — R228 100R — C555 10n 16V — R419 22k — HP_L
DSP_CH2_R — R229 100R — C554 10n 16V — R420 22k — HP_R
DSP_CH4_L — R224 100R — C550 10n 16V — R415 22k — LINE_OUT_L

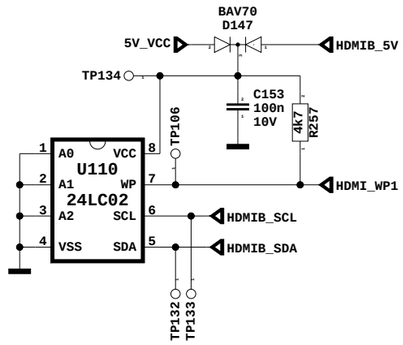
DSP_CH1_L — R227 100R — C553 10n 16V — R418 22k — MAIN_L
DSP_CH1_R — R226 100R — C552 10n 16V — R417 22k — MAIN_R
DSP_CH3_L — R223 100R — C549 10n 16V — R414 22k — SC1_L
DSP_CH3_R — R222 100R — C548 10n 16V — R413 22k — SC_1_R

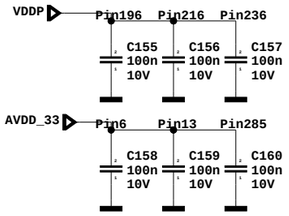
Place close to Paulo
DSP_CH4_R — R225 100R — C551 10n 16V — R416 22k — LINE_OUT_R

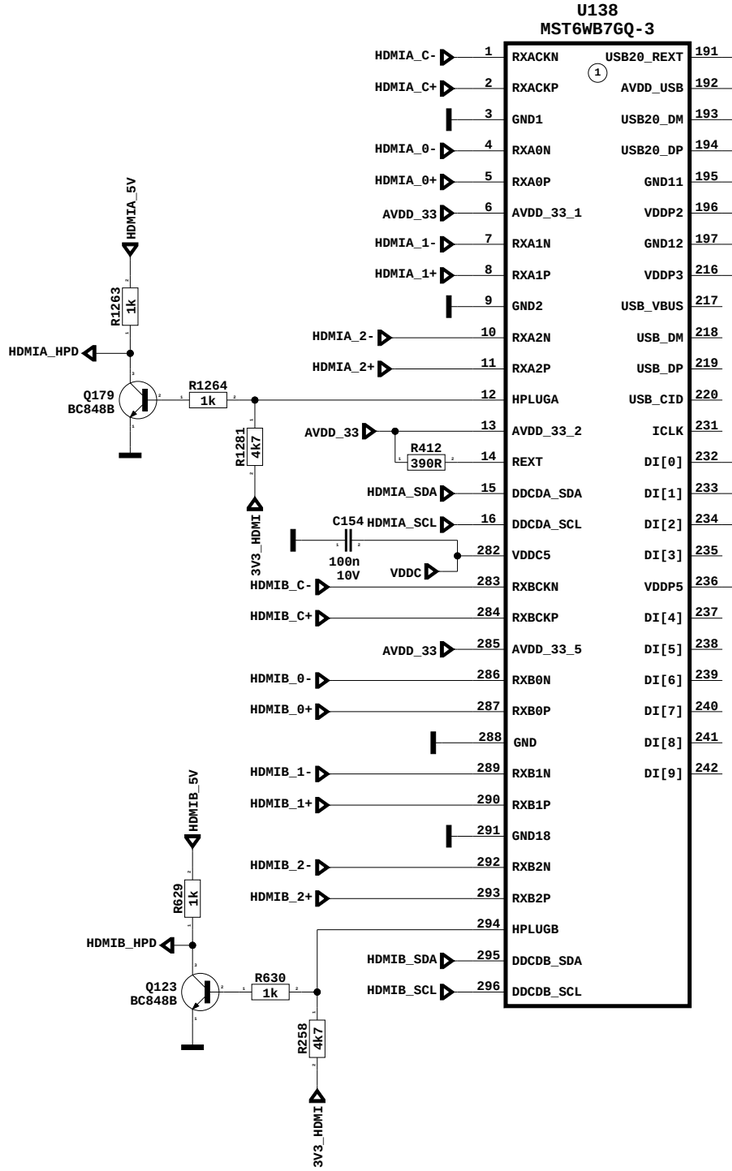
AUDIO OUTPUT FILTERS

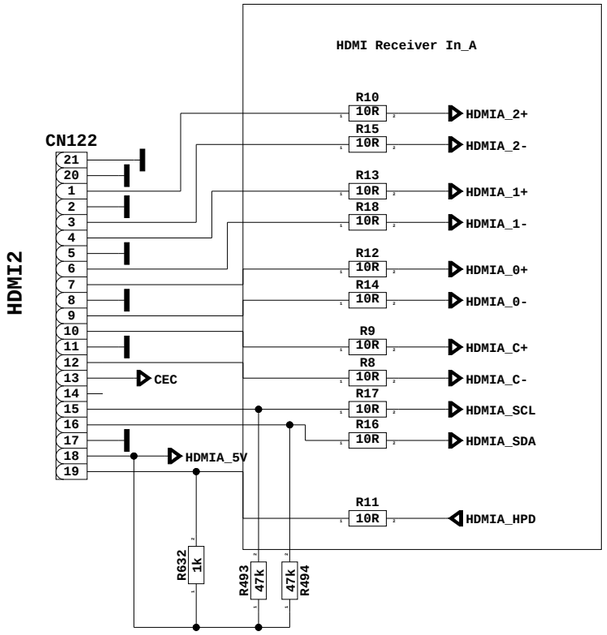
VESTEL	PROJECT NAME : 17mb37		A3
SCH NAME :<DRAWING NAME HERE>		SHEET: 3 OF: 18	
DRAWN BY :<YOUR NAME HERE>		14-10-2009 09:10	

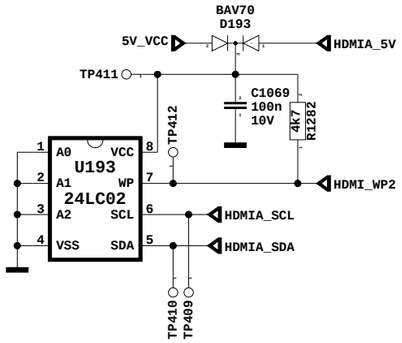




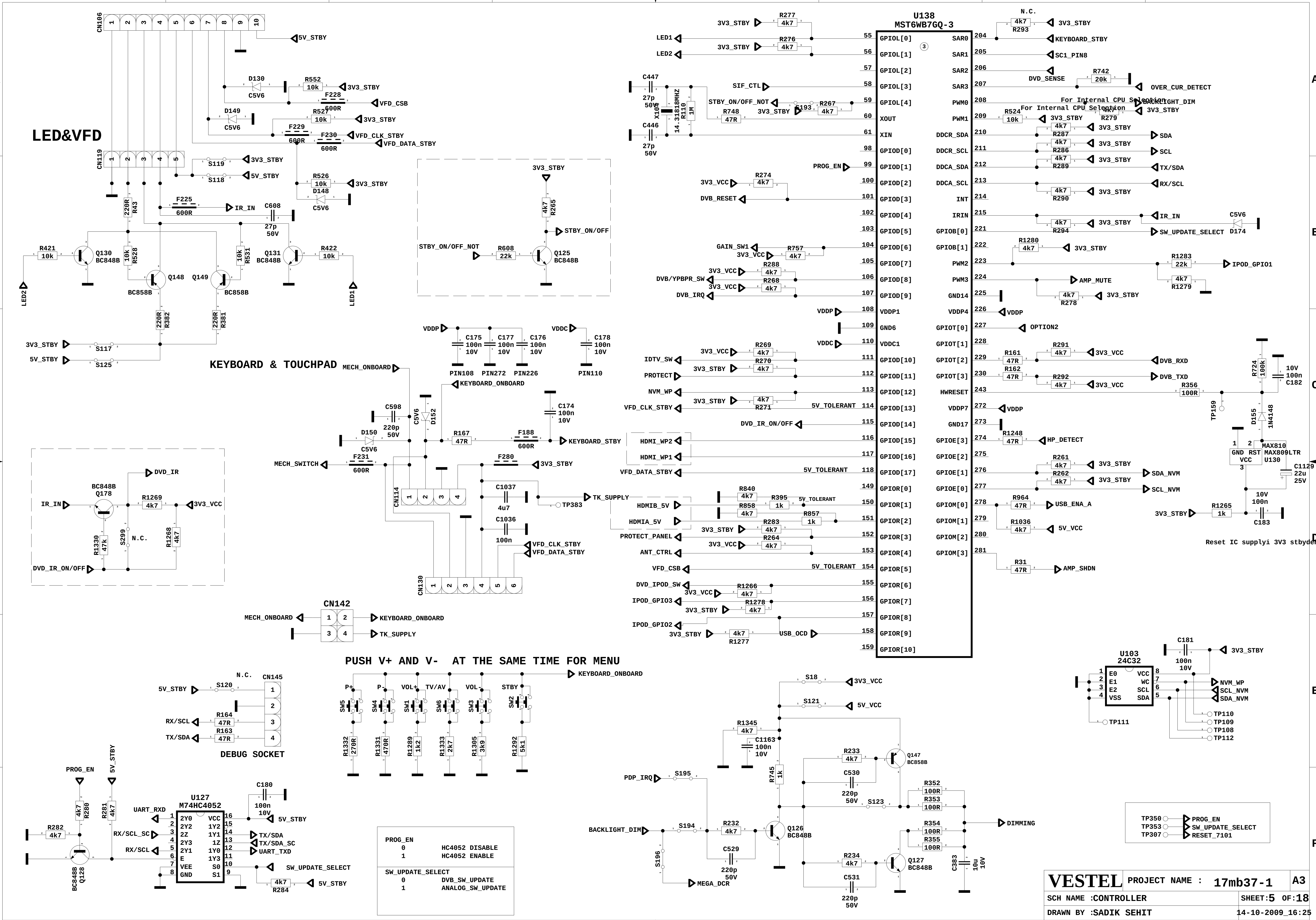




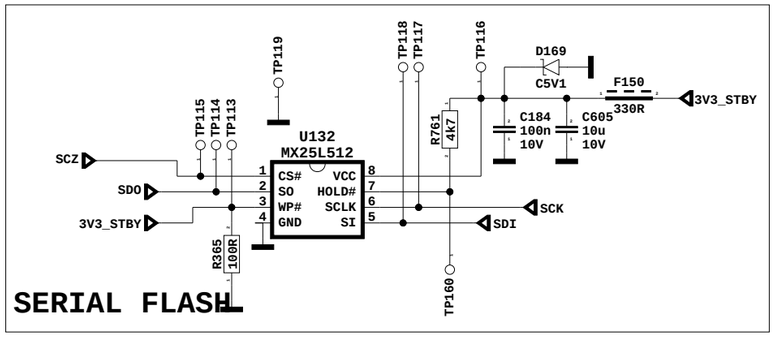


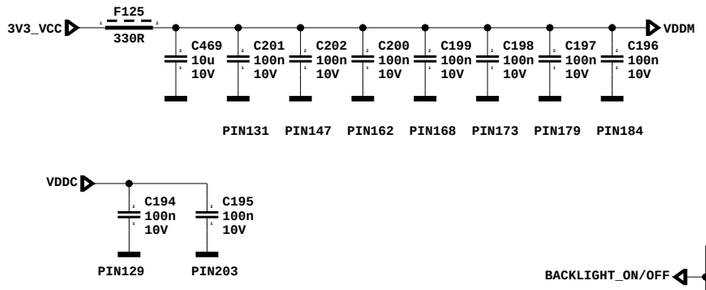


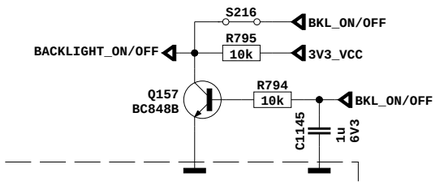
VESTEL	PROJECT NAME : 17mb37	A3
SCH NAME :HDMI&USB	SHEET:4 OF:18	
DRAWN BY :SADIK SEHIT	14-10-2009_09:10	

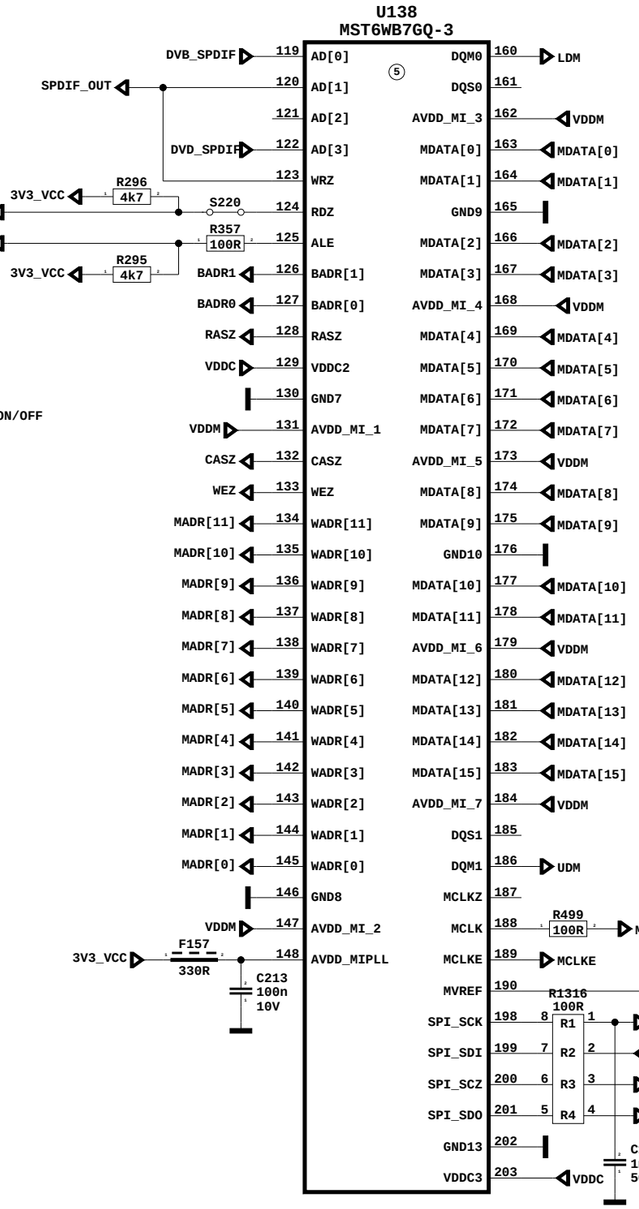


LED&VFD
KEYBOARD & TOUCHPAD
PUSH V+ AND V- AT THE SAME TIME FOR MENU
DEBUG SOCKET
U138
MST6WB7GQ-3
U127
M74HC4052
U103
24C32
U130
MAX810
MAX809LTR
CN106
CN119
CN114
CN130
CN142
CN145
For Internal CPU Selection
Reset IC supplyi 3V3 stbyden
PROG_EN
0 HC4052 DISABLE
1 HC4052 ENABLE
SW_UPDATE_SELECT
0 DVB_SW_UPDATE
1 ANALOG_SW_UPDATE
TP350 PROG_EN
TP353 SW_UPDATE_SELECT
TP307 RESET_7101
VESTEL
PROJECT NAME : 17mb37-1
A3
SCH NAME :CONTROLLER
SHEET:5 OF:18
DRAWN BY :SADIK SEHIT
14-10-2009_16:25



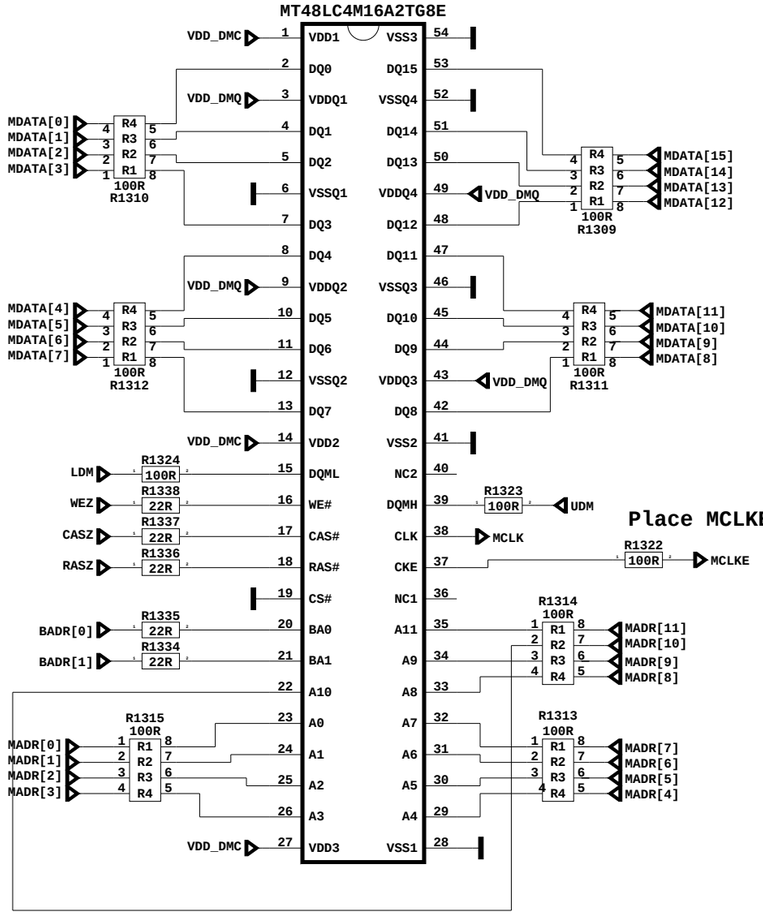




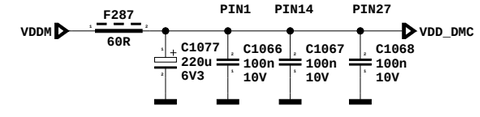


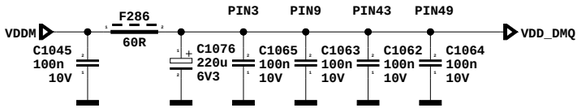
MEMORY

8MB SDRAM



Place MCLKE Clock resistor close to MSTAR Pin

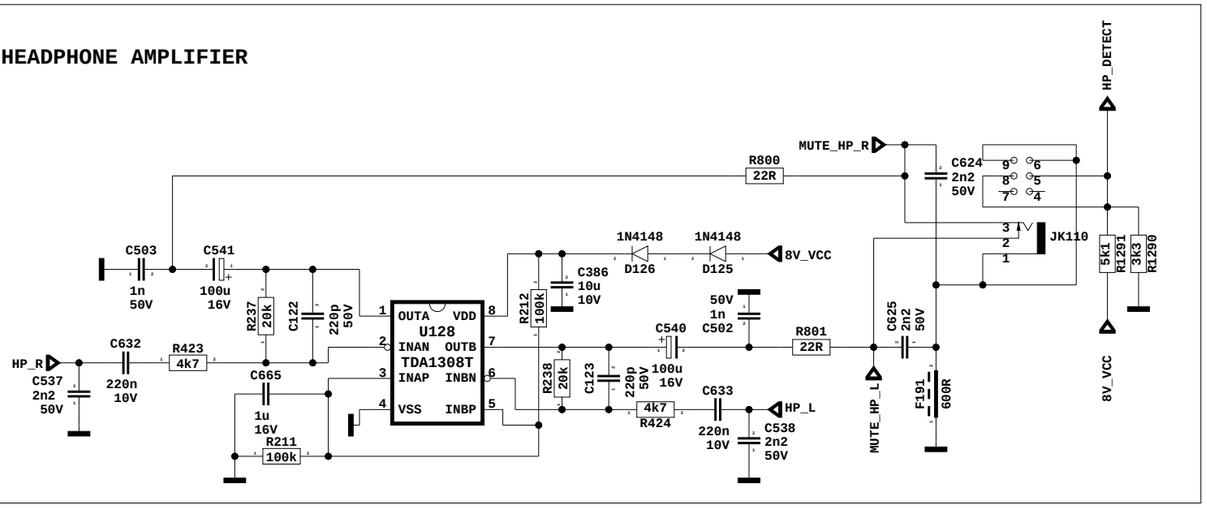




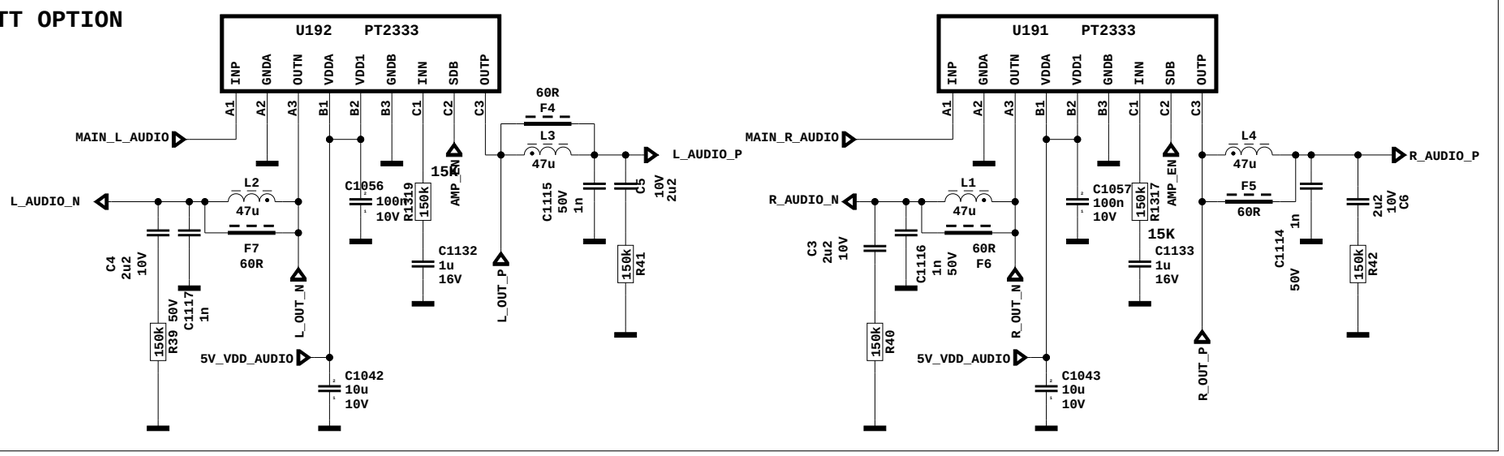
WARNING!!!DON'T USE VIA FOR MCLK AND DATA SIGNALS

VESTEL	PROJECT NAME : 17mb37	A3
SCH NAME :MEMORY INTERFACE	SHEET:6 OF:18	
DRAWN BY :ÖNDER GENÇ	14-10-2009_09:10	

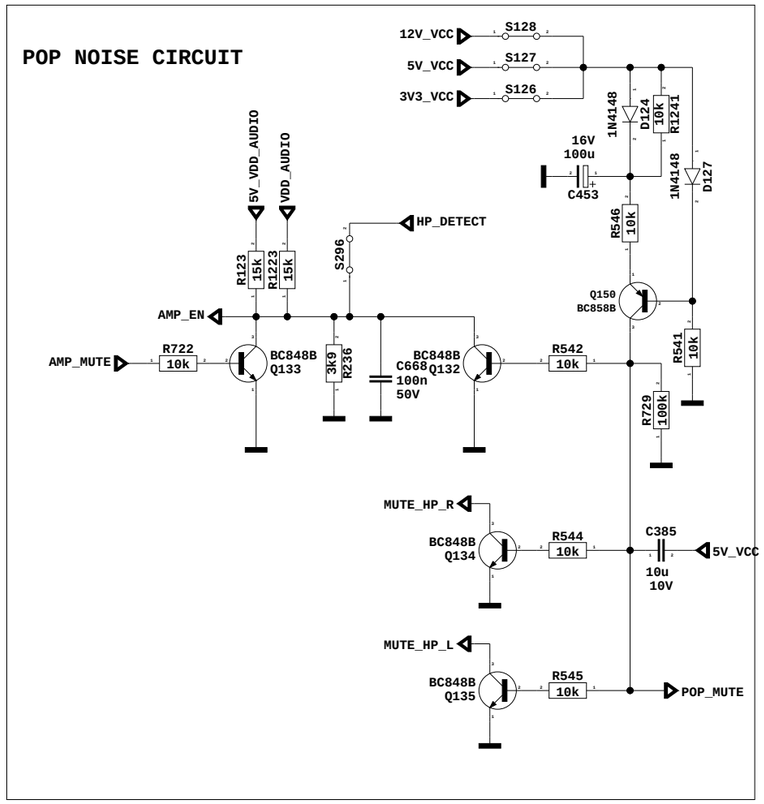
HEADPHONE AMPLIFIER

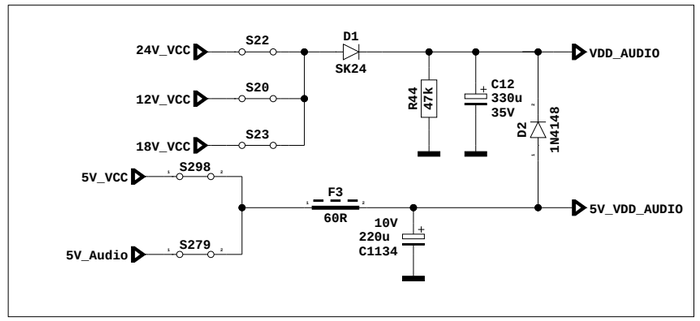


2.5 WATT OPTION

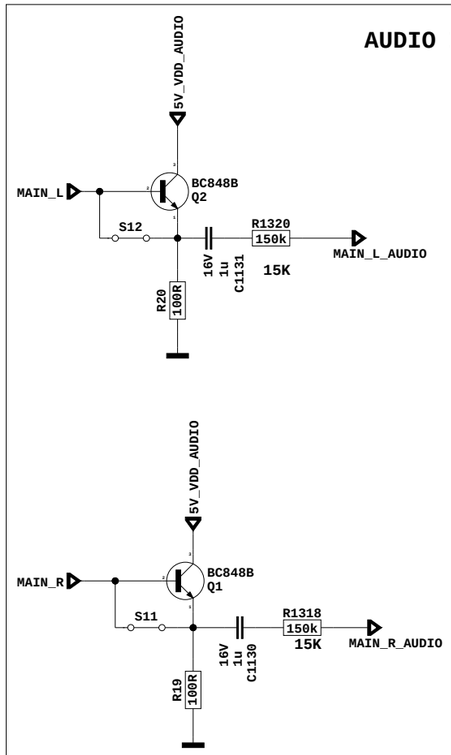


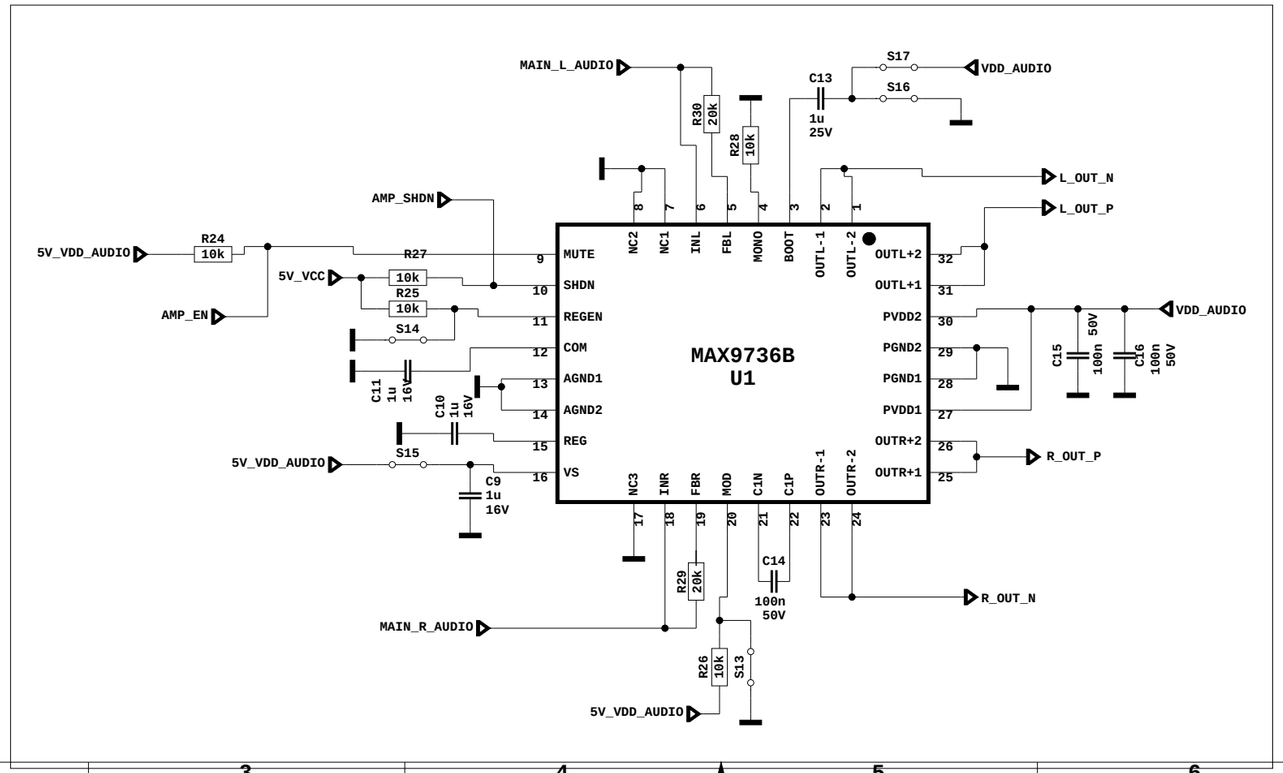
POP NOISE CIRCUIT

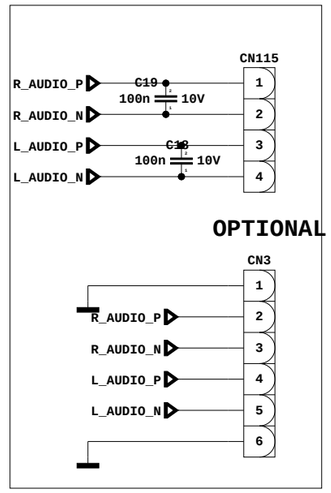




AUDIO INPUTS







VESTEL	PROJECT NAME : 17mb37	A3
SCH NAME :AUDIO		SHEET:7 OF:18
DRAWN BY :SADIK SEHIT		15-10-2009_16:06

DVB-T DEMODULATOR

U152
STV0362

DVB-C DEMODULATOR

U109
STV0297E

U174
TS431AIL

Q176
BC846B

BCP56-16
Q175

D166
BA159

U182
FSA3157

Q171
BC847B

Q170
BC847B

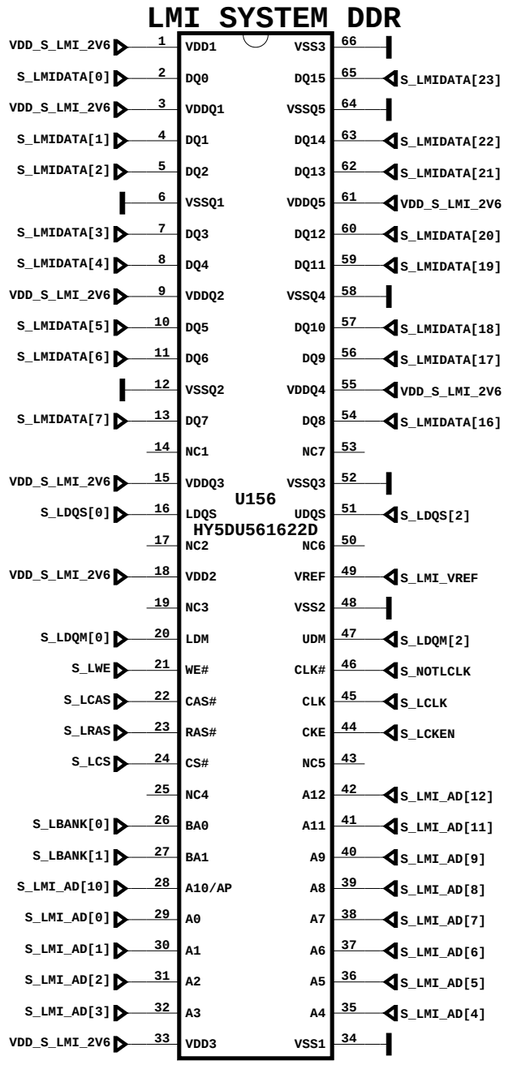
BC817-25
Q103

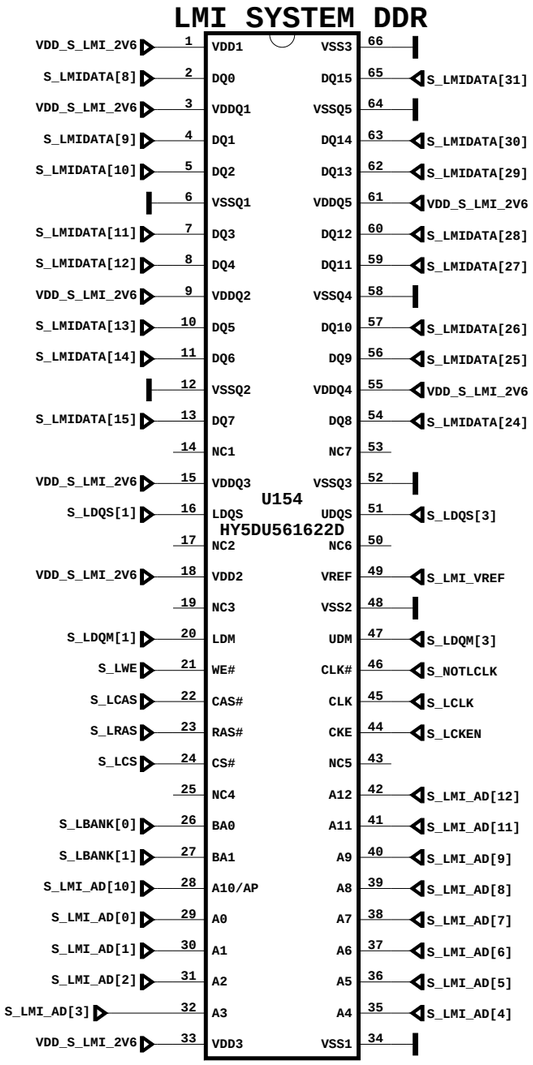
X108
27MHz

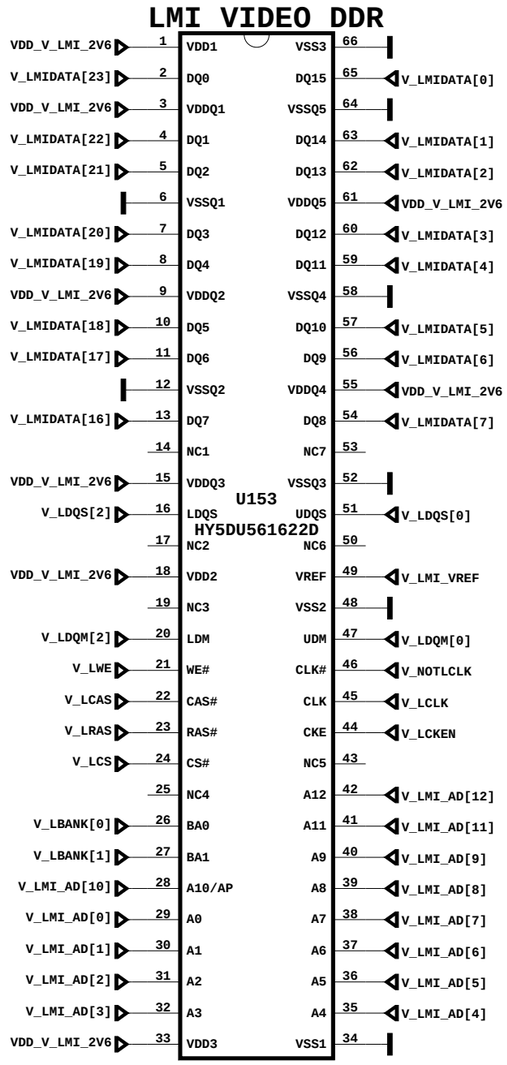
X101
27MHZ

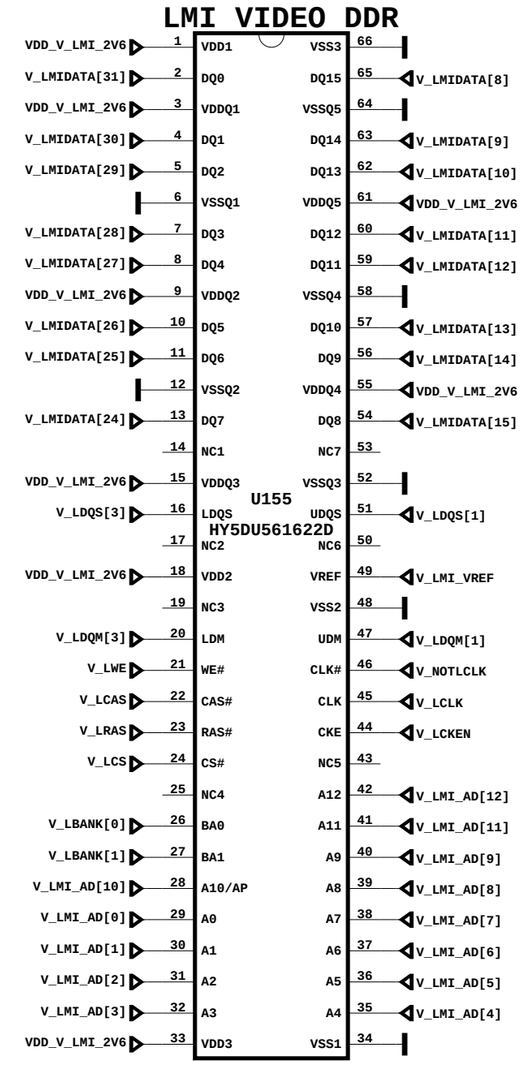
place this cap close to pin#56

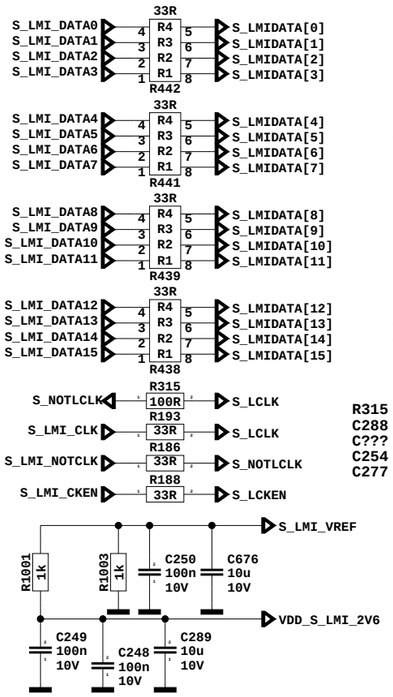
VESTEL	PROJECT NAME 17mb37		A3
SCH NAME :DVB COFDM & QAM		SHEET:8	OF:18
DRAWN BY :ERTUG BAL		14-10-2009_09:10	

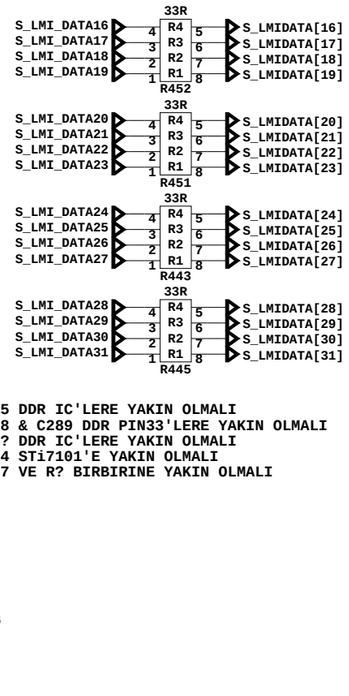


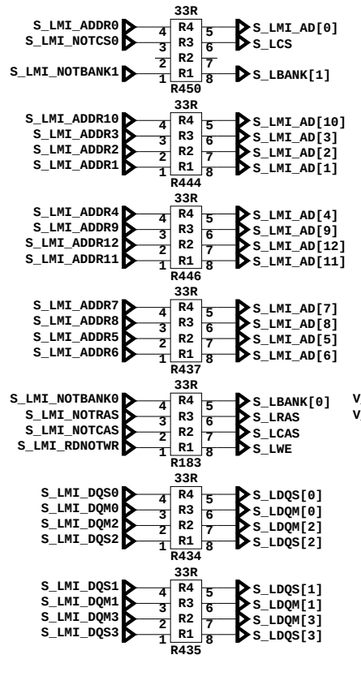


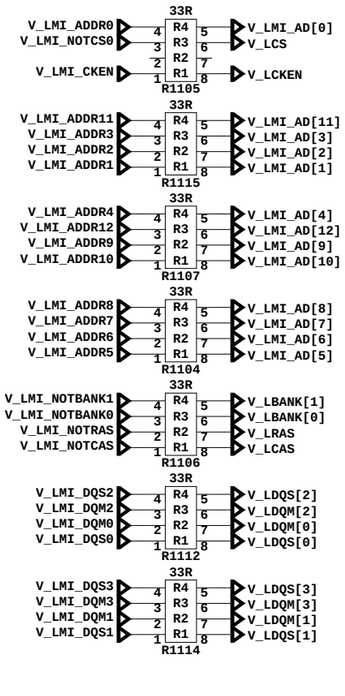


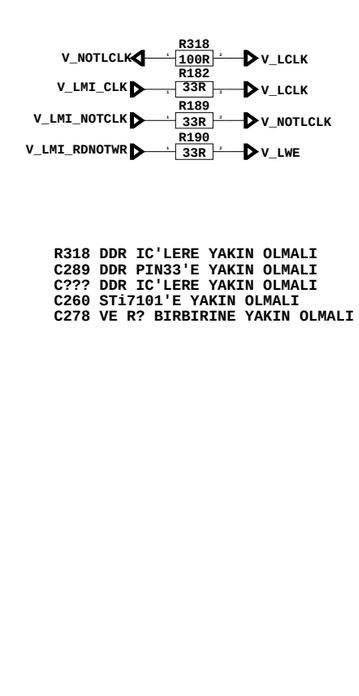


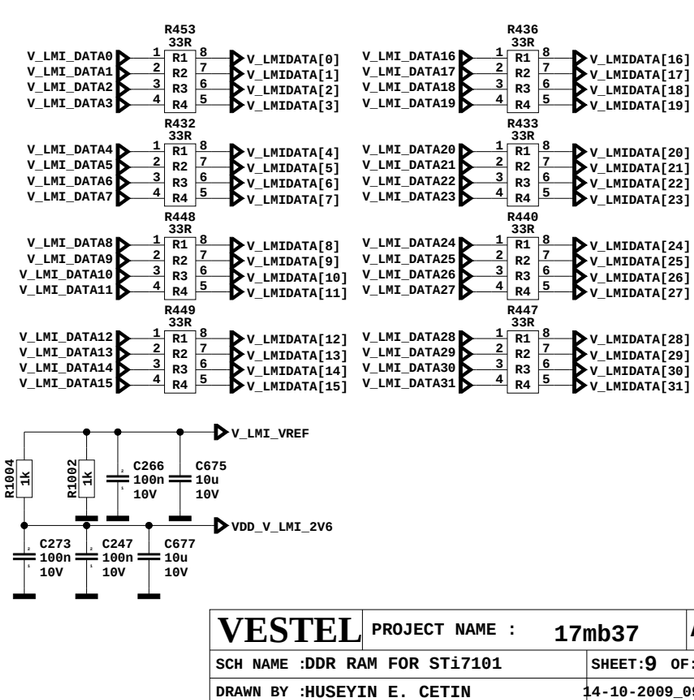




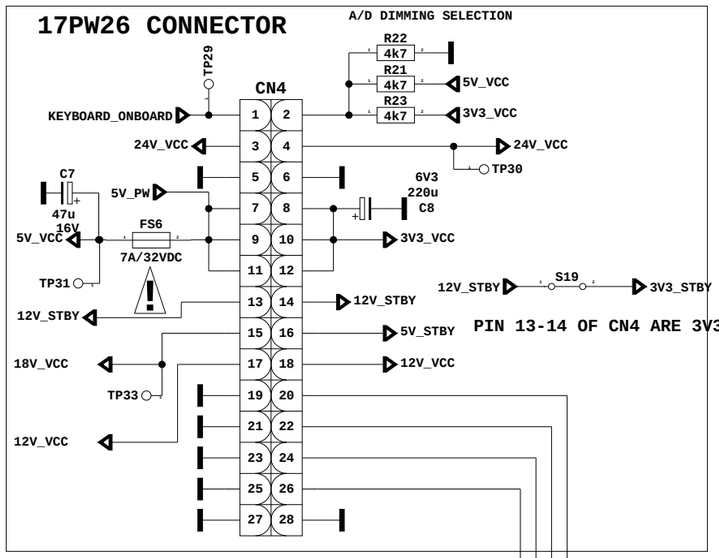


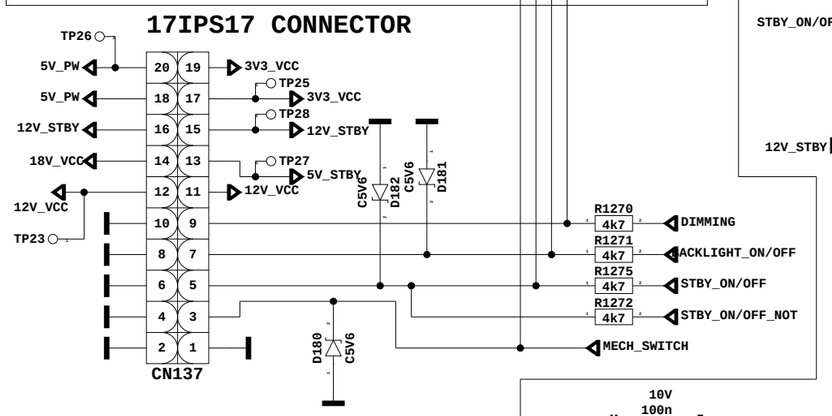


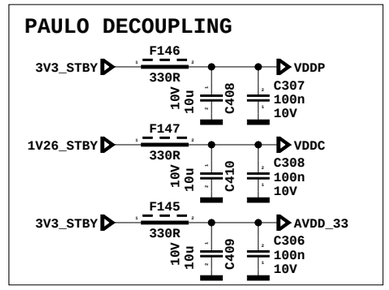


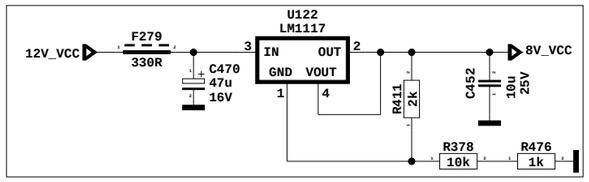


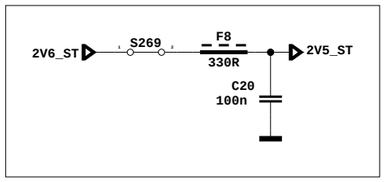
VESTEL	PROJECT NAME : 17mb37	A3
SCH NAME :DDR RAM FOR STi7101	SHEET:9 OF:18	
DRAWN BY :HUSEYIN E. CETIN	14-10-2009_09:10	

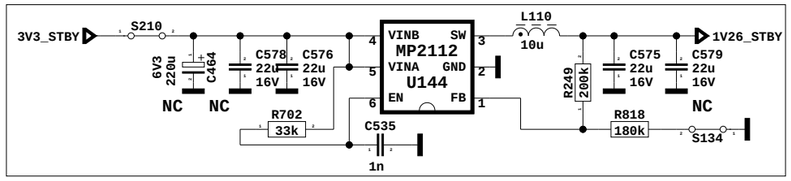


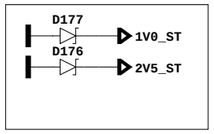


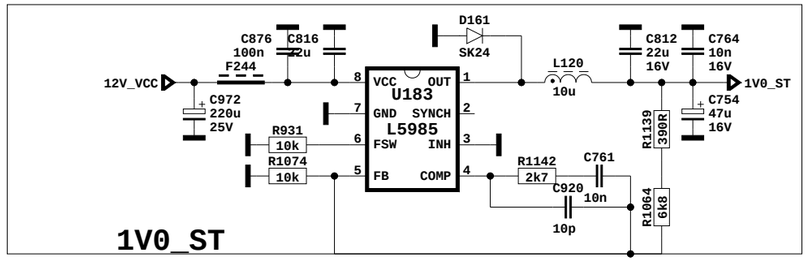


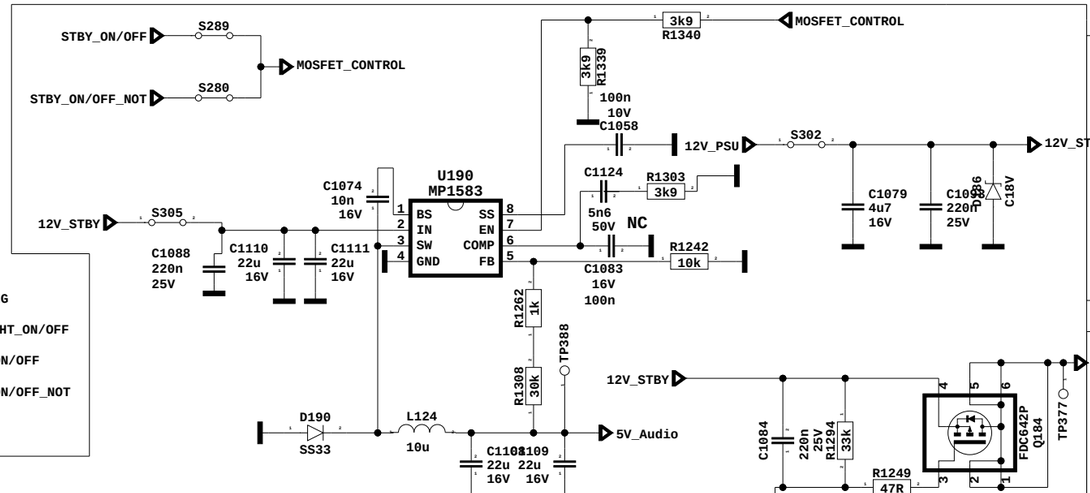


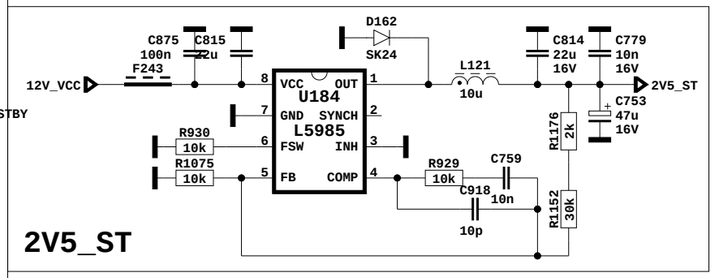


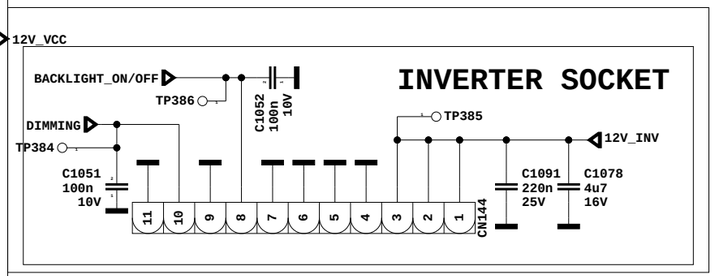


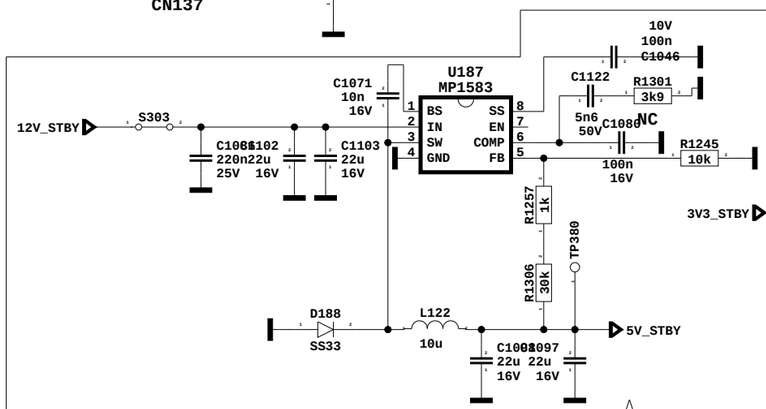


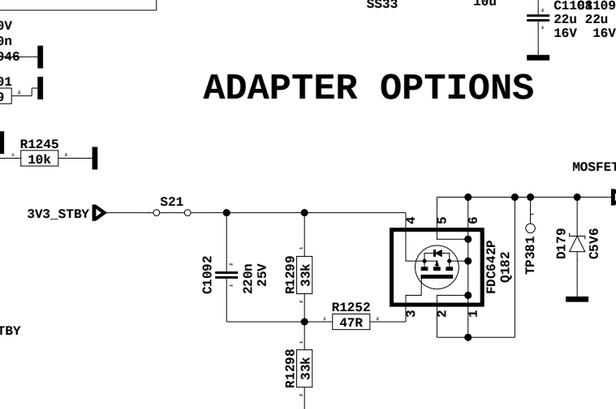


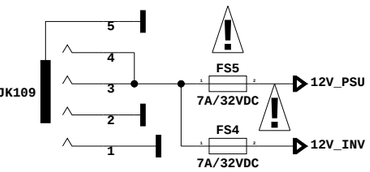


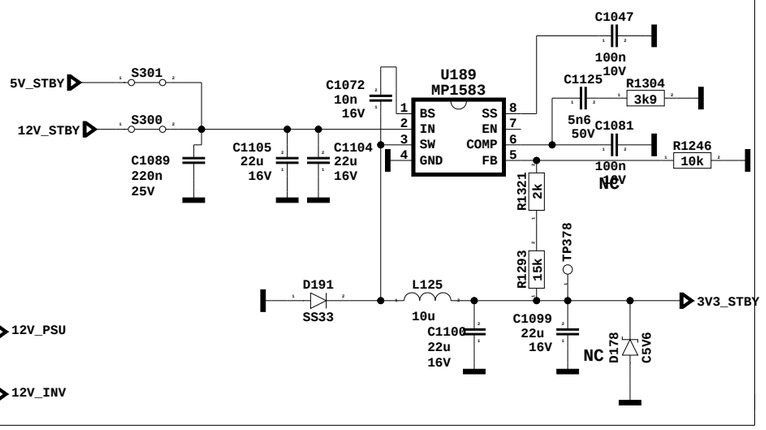


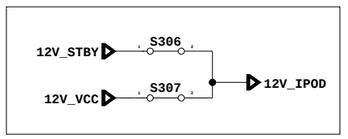


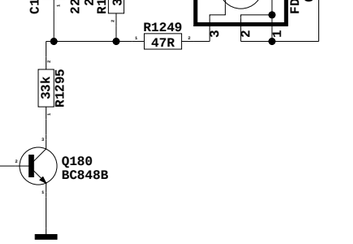


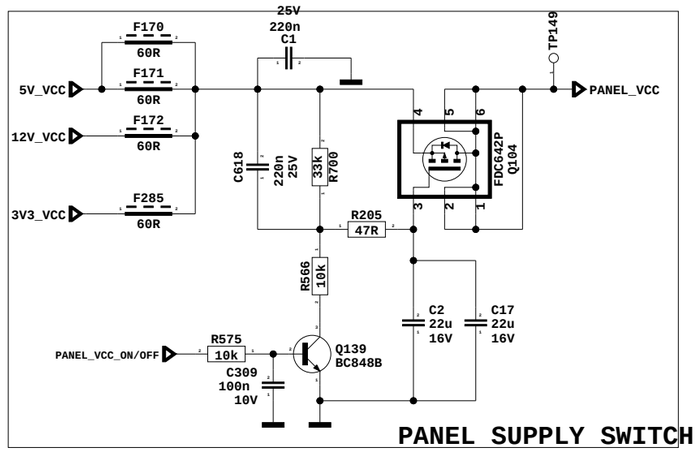












VESTEL	PROJECT NAME : 17mb37		A3
SCH NAME :POWER		SHEET:10 OF:18	
DRAWN BY :SADIK SEHIT		15-10-2009_15:59	

U138
MST6WB7GQ-3

GND15 244
VDDC4 245 ◁ VDDC
LVA4P 246
LVA4M 247
LVA3P 248 ▷ RX_A_3_P
LVA3M 249 ▷ RX_A_3_N
LVACKP 250 ▷ RX_A_CLK_P
LVACKM 251 ▷ RX_A_CLK_N
LVA2P 252 ▷ RX_A_2_P
LVA2M 253 ▷ RX_A_2_N
LVA1P 254 ▷ RX_A_1_P
LVA1M 255 ▷ RX_A_1_N
LVA0P 256 ▷ RX_A_0_P
LVA0M 257 ▷ RX_A_0_N
VDDP6 258 ◁ VDDP
GND16 259
LVB4P 260
LVB4M 261
LVB3P 262 ▷ RX_B_3_P
LVB3M 263 ▷ RX_B_3_N
LVBCKP 264 ▷ RX_B_CLK_P
LVBCKM 265 ▷ RX_B_CLK_N
LVB2P 266 ▷ RX_B_2_P
LVB2M 267 ▷ RX_B_2_N
LVB1P 268 ▷ RX_B_1_P
LVB1M 269 ▷ RX_B_1_N
LVB0P 270 ▷ RX_B_0_P
LVB0M 271 ▷ RX_B_0_N

C311 100n 10V

19" TO 22" FFC OPTIONS

CN138

RX_B_0_N 1
RX_B_0_P 2
RX_B_1_N 3
RX_B_1_P 4
RX_B_2_N 5
RX_B_2_P 6
7
RX_B_CLK_N 8
RX_B_CLK_P 9
RX_B_3_N 10
RX_B_3_P 11
RX_A_0_N 12
RX_A_0_P 13
14
RX_A_1_N 15
RX_A_1_P 16
17
RX_A_2_N 18
RX_A_2_P 19
RX_A_CLK_N 20
RX_A_CLK_P 21
RX_A_3_N 22
RX_A_3_P 23
24
S295 25
PANEL_VCC ▷ S290 26
S291 27
PANEL_VCC 28
29
30

PANEL_VCC = 5V

LVDS CABLE

TP402

CN139

RX_B_0_N 1 2
TP396
RX_B_0_P 3 4
TP392
RX_B_1_N 5 6
TP404
RX_B_1_P 7 8
TP390
RX_B_2_N 9 10
TP408
RX_B_2_P 11 12
13 14
TP407
RX_B_CLK_N 15 16
TP389
RX_B_CLK_P 17 18
TP403
RX_B_3_N 19 20 ◁ PANEL_VCC
TP391
RX_B_3_P 21 22
TP401
RX_A_0_N 23 24
TP394
RX_A_0_P 25 26
27 28
TP395
RX_A_1_N 29 30
RX_A_1_P 31 32 ▷ S288
BACKLIGHT_ON/OFF TP405 TP400 33 34 ◁ BACKLIGHT_ON/OFF
TP406 RX_A_2_N 35 36
RX_A_2_P 37 38 ▷ S286
RX_A_CLK_N 39 40
RX_A_CLK_P 41 42 ◁ OPTION1
TP397
RX_A_3_N 43 44 ◁ OPTION2
TP399
RX_A_3_P 45 46 ◁ OPTION3
TP393
47 48
MEGA_DCR 49 50

CN140

PANEL_VCC
RX_B_3_P 1 2
RX_A_0_N 3 4
RX_A_0_P 5 6
7 8
RX_A_1_N 9 10
RX_A_1_P 11 12
13 14
BACKLIGHT_ON/OFF
15 16
RX_A_2_N 17 18
RX_A_2_P 19 20
RX_A_CLK_N 21 22 ◁ OPTION1
RX_A_CLK_P 23 24 ◁ OPTION2
RX_A_3_N 25 26 ◁ OPTION3
RX_A_3_P 27 28
29 30

S285
10k R1244 ◁ 3V3_VCC
10k R1243 ◁ 3V3_VCC
▷ PDP_IRQ
S288
S286
S284
S287
S283

SHORT CCT PROTECTION

PROTECT_PANEL
Q137 BC848B
R708 33k ◁ PANEL_VCC
10k R571

R706 33k ◁ 8V_VCC
10k R569
D135 BAW56
5V_TUN
3V3_VCC
D136 BAW56
5V_VCC
D137 BAW56
D3 BAW56

3V3_STBY
R565 10k
PROTECT
TP150
Q151 BC858B
R564 10k
Q136 BC848B
R563 10k
R562 10k

R705 33k ◁ 12V_VCC
10k R568
R37 33k ◁ 24V_VCC
10k R32
S228 ◁ LOWER_SUP

LOWER_SUP
Q163 BC848B
3V3_VCC
R912 10k
1k R1000
Q162 BC848B
R914 10k
R913 10k

D159 BAW56
1k R1259
1k R1260 ▷ 2V6_ST
1k R1255 ▷ 2V5_ST
D158 BAW56
1k R1256 ▷ 1V0_FE
▷ 1V0_ST

LOWER SUPPLY SHORT CCT PROTECTION

PANEL VCC = 5V/12V

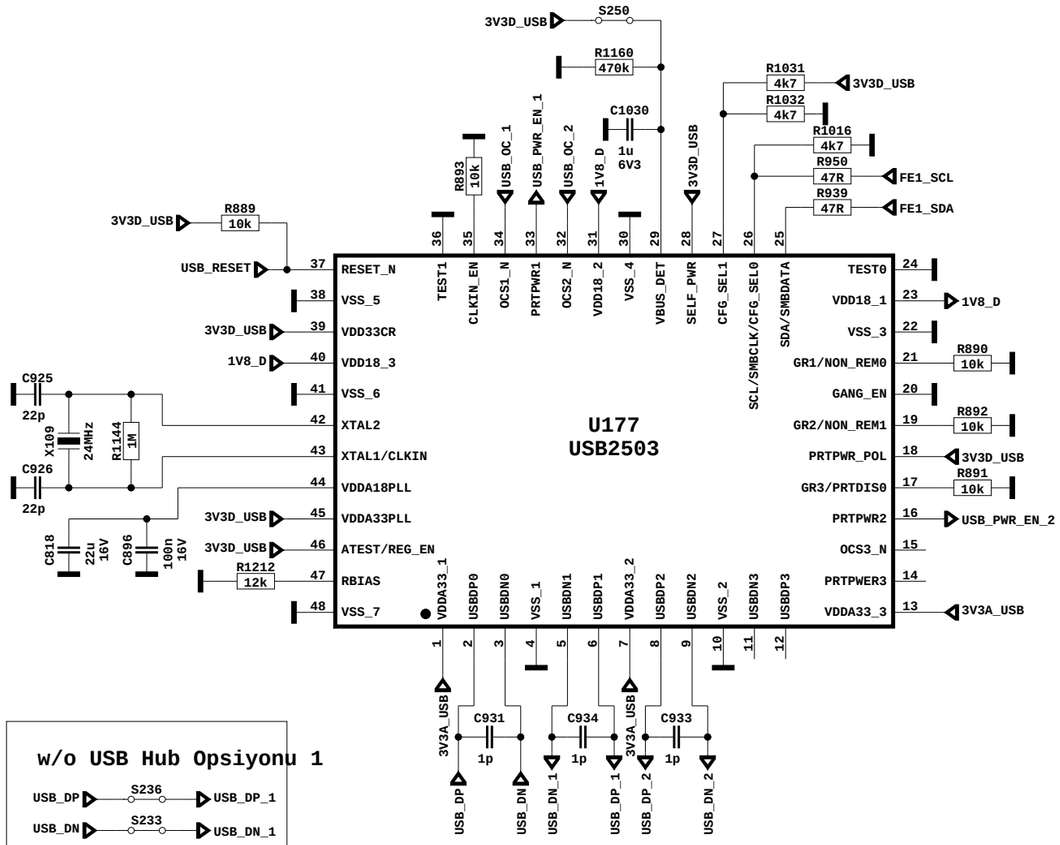
PANEL_VCC
MEGA_DCR S6
OPTION2 10k R1 S5
3V3_VCC S8
3V3_VCC 10k R2
OPTION1
PDP_IRQ S9
RX_A_3_P S1
RX_A_3_N S3
RX_A_CLK_P S4
RX_A_CLK_N
RX_A_2_P
RX_A_2_N
RX_A_1_P
RX_A_1_N
RX_A_0_P
RX_A_0_N
PANEL_VCC R3 10k S2
R4 10k 3V3_VCC
R5 10k 330R F1
PANEL_VCC
OPTION3
10k R7 3V3_VCC
10k R6 330R F2
PANEL_VCC

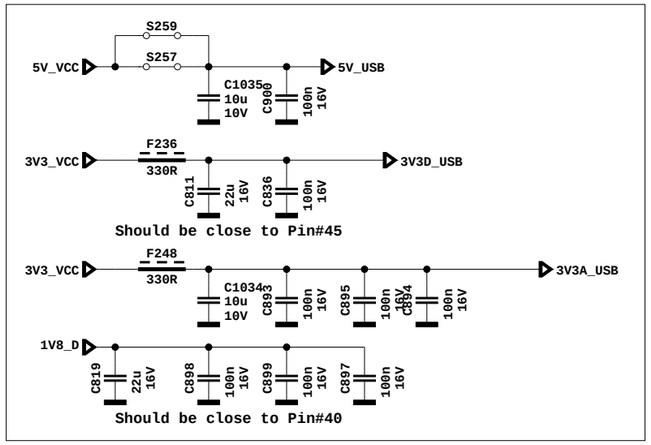
CN2: 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

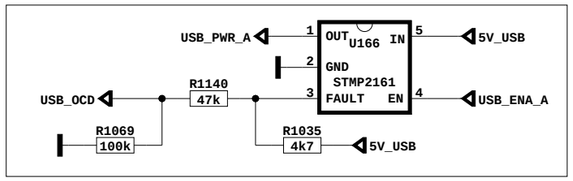
CN1: 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

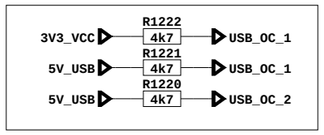
PANEL_VCC = 5V/12V

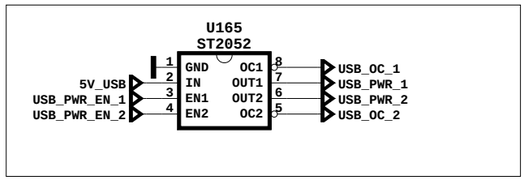
VESTEL	PROJECT NAME : 17mb37	A3
SCH NAME :LVDS INTERFACE	SHEET:11OF:18	
DRAWN BY :SADIK SEHIT	14-10-2009_09:09	

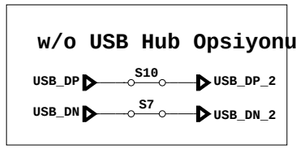


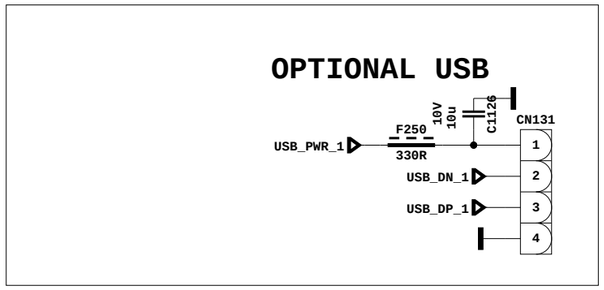


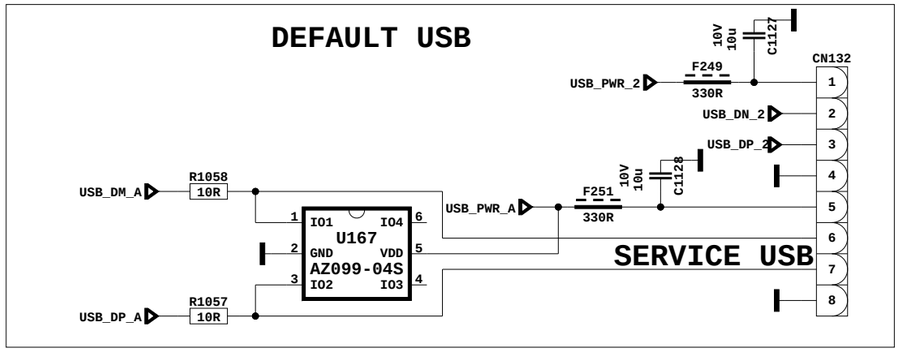




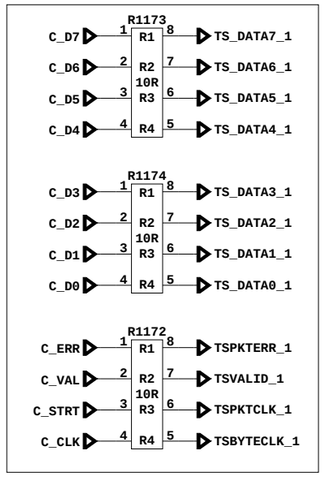


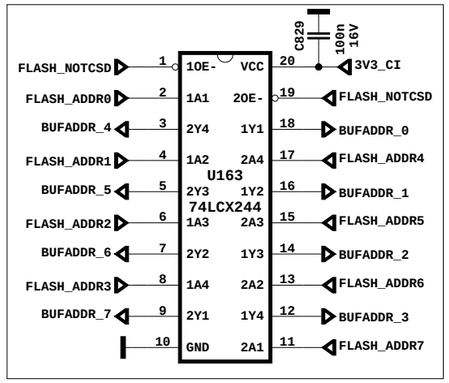


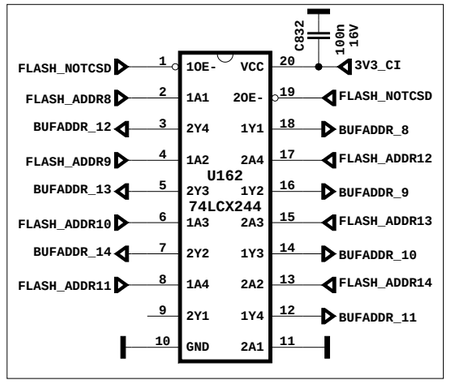


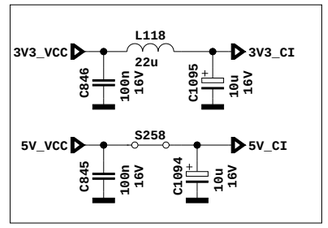


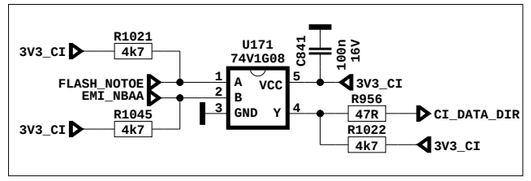
VESTEL	PROJECT NAME : 17mb37	A3
SCH NAME :USB		SHEET:12OF:18
DRAWN BY :SADIK SEHIT		14-10-2009_09:09

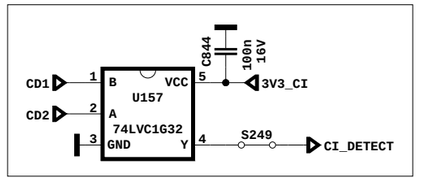


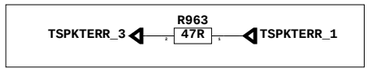


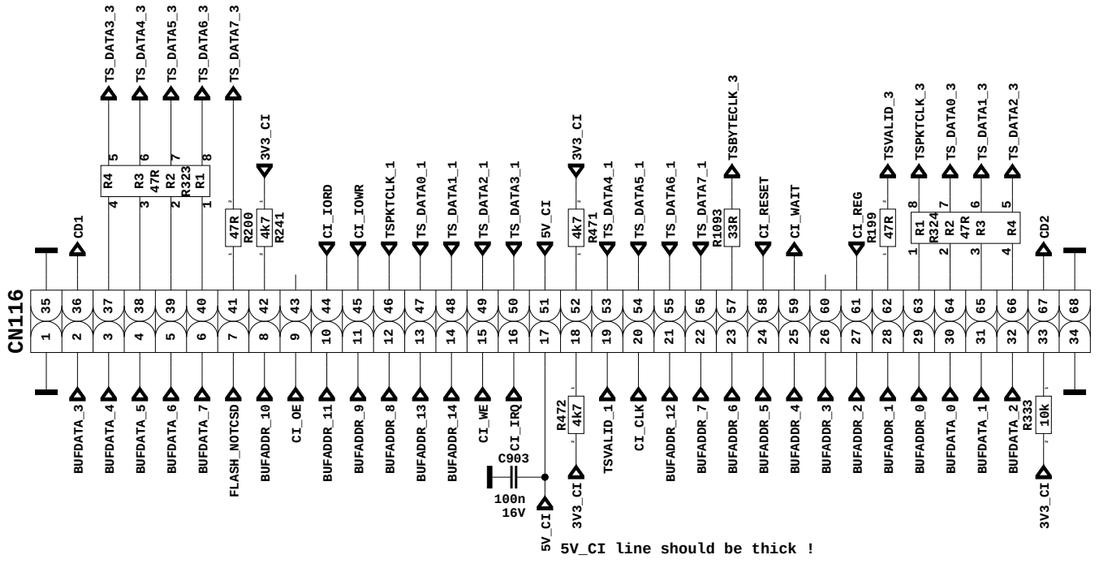


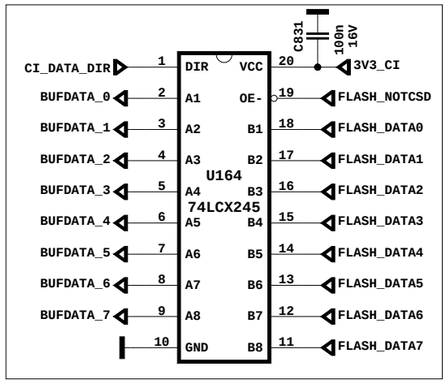


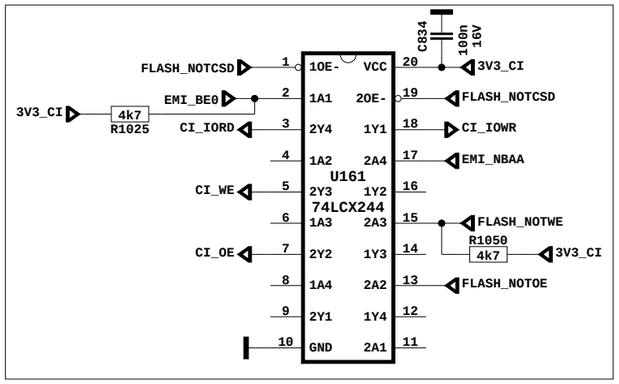


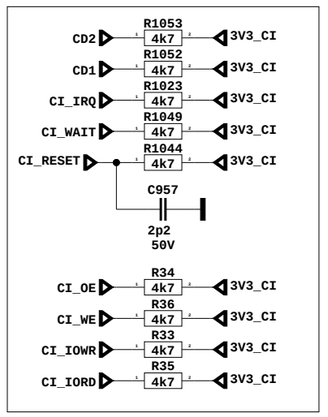


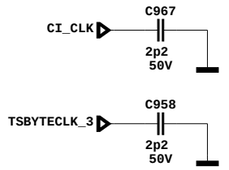


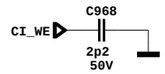




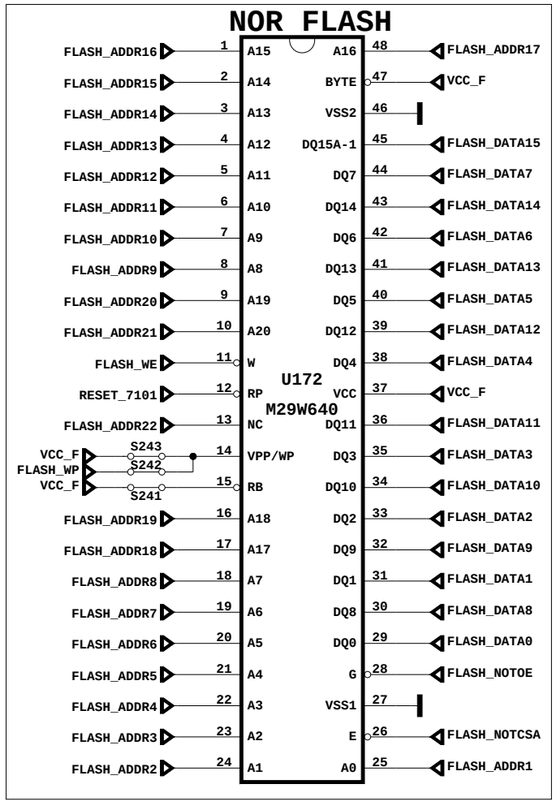


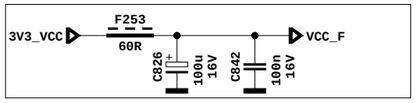


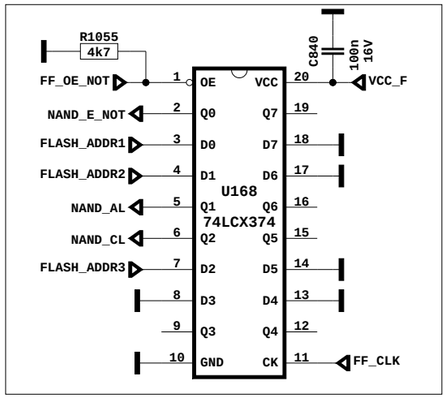


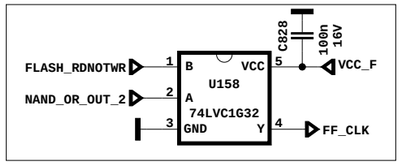


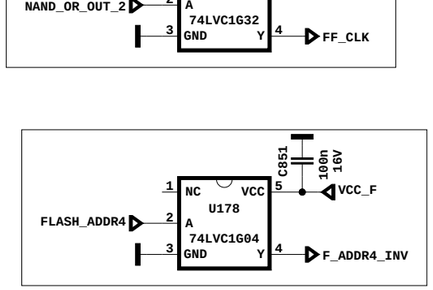
VESTEL	PROJECT NAME 17mb37	A3
SCH NAME :STi7101 NOR FLASH & CI		SHEET:13 OF:18
DRAWN BY :ERTUG BAL		14-10-2009_09:10

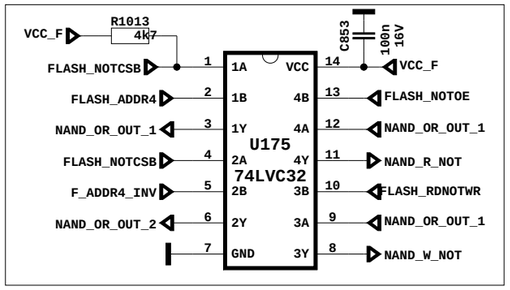


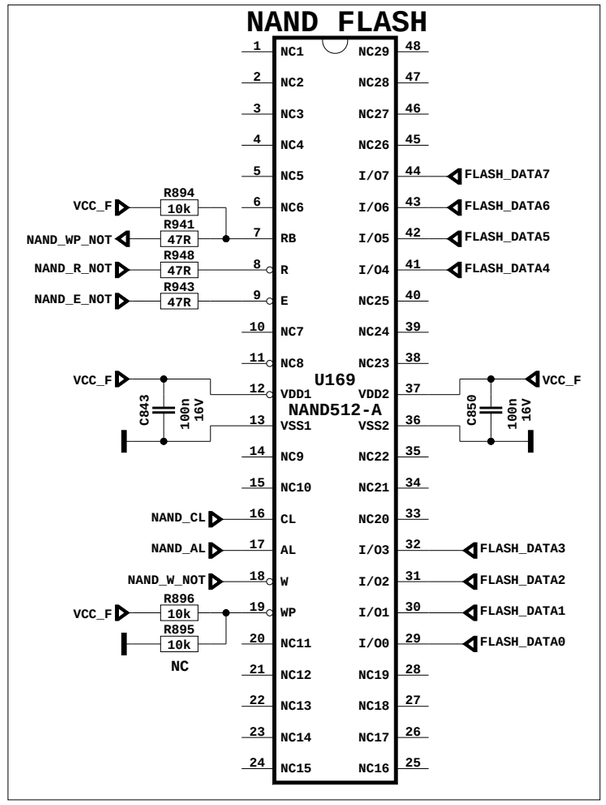


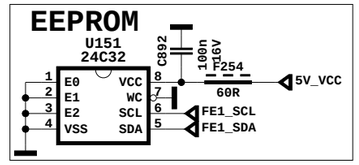


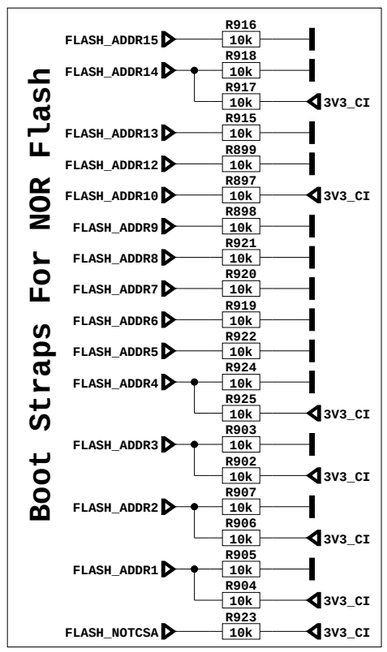


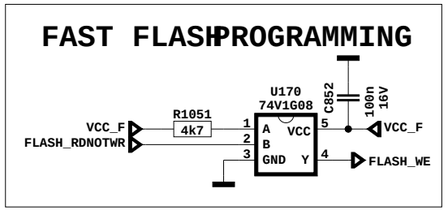




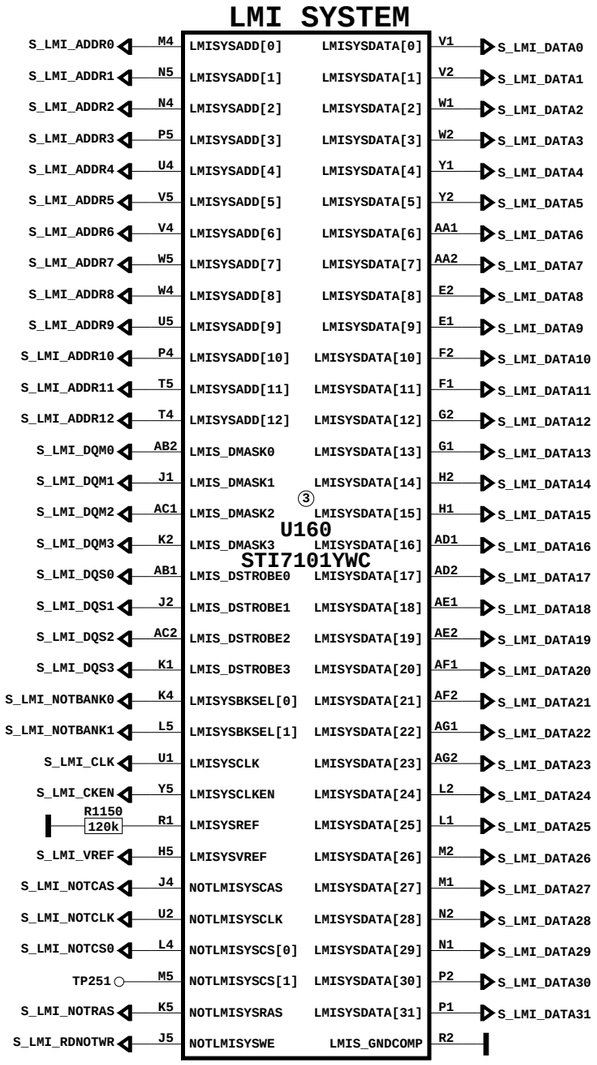


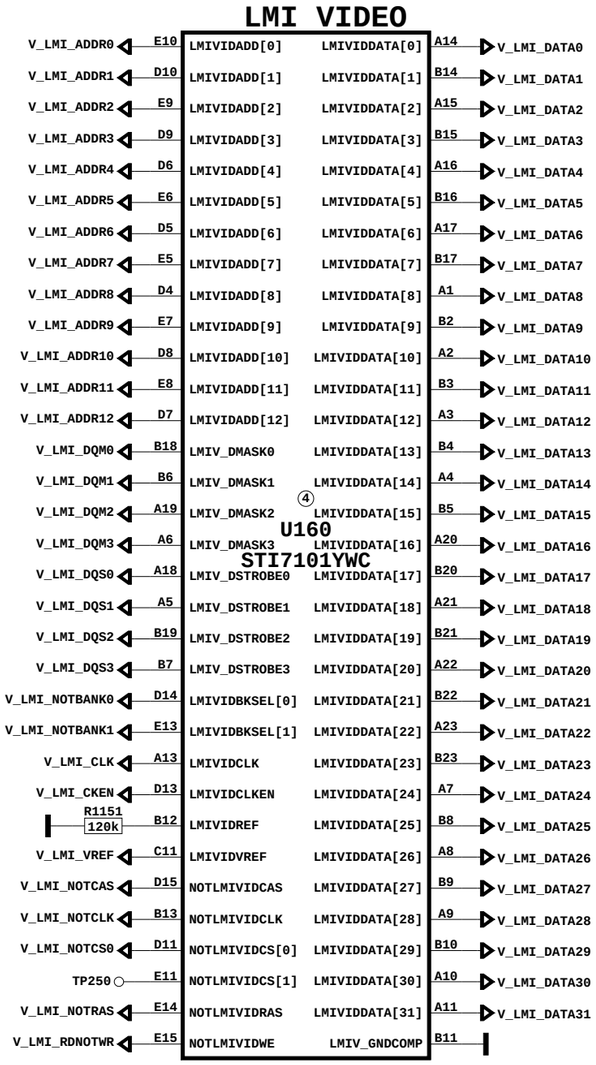


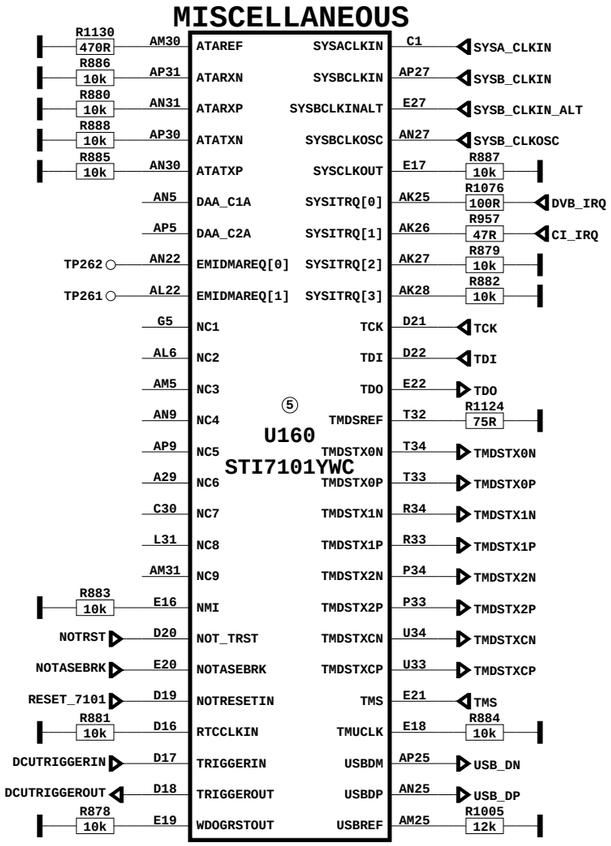


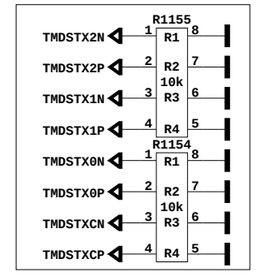


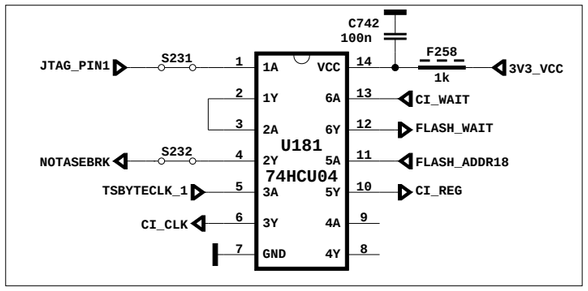
VESTEL	PROJECT NAME 17mb37	A3
SCH NAME :STi7101 FLASH & EEPROM		SHEET:14OF:18
DRAWN BY :ERTUG BAL		14-10-2009_09:10

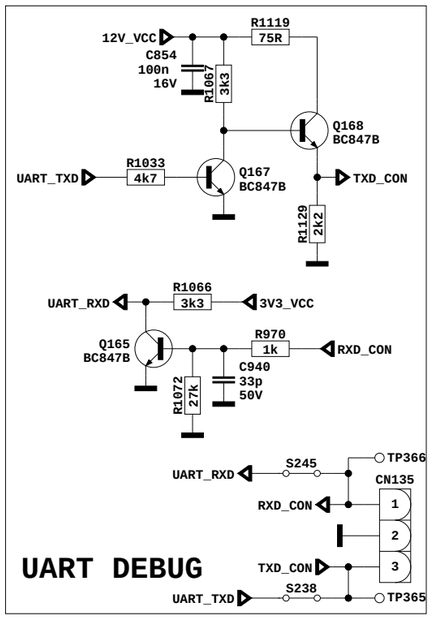


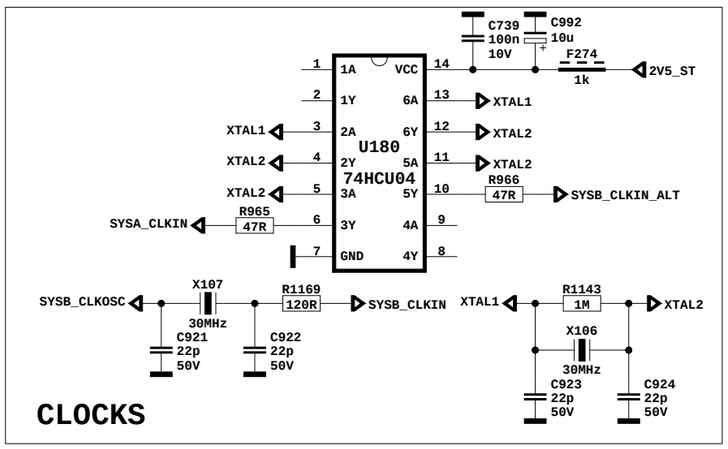


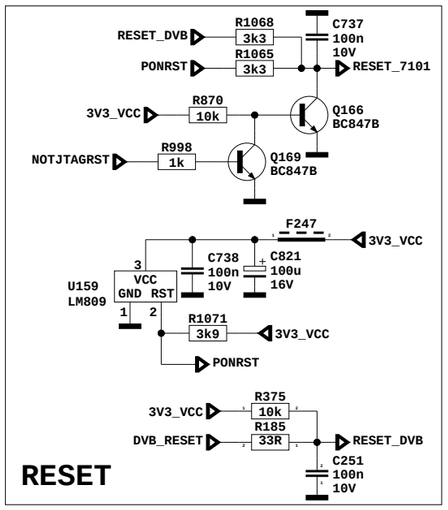


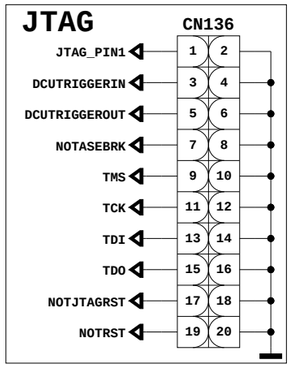




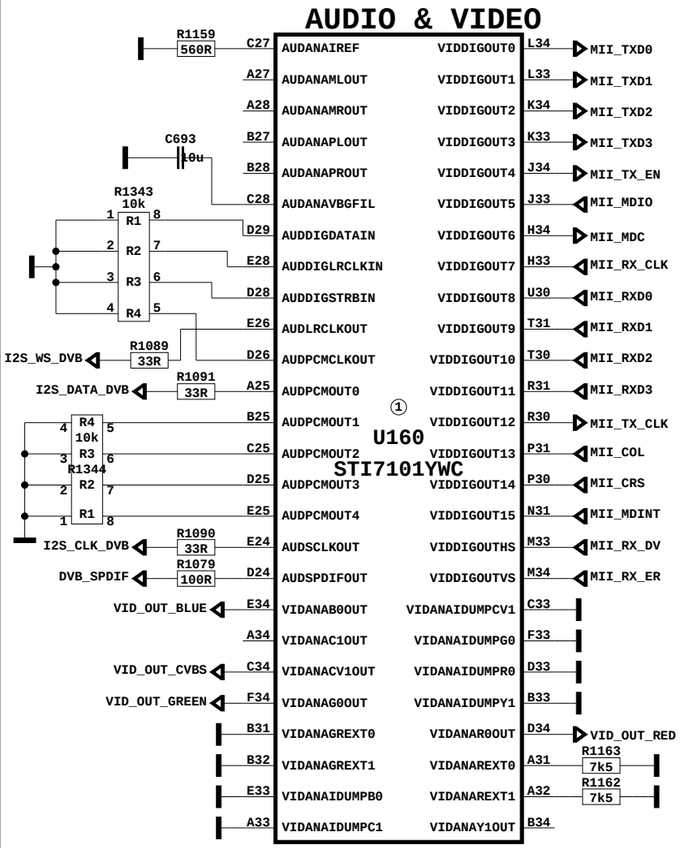


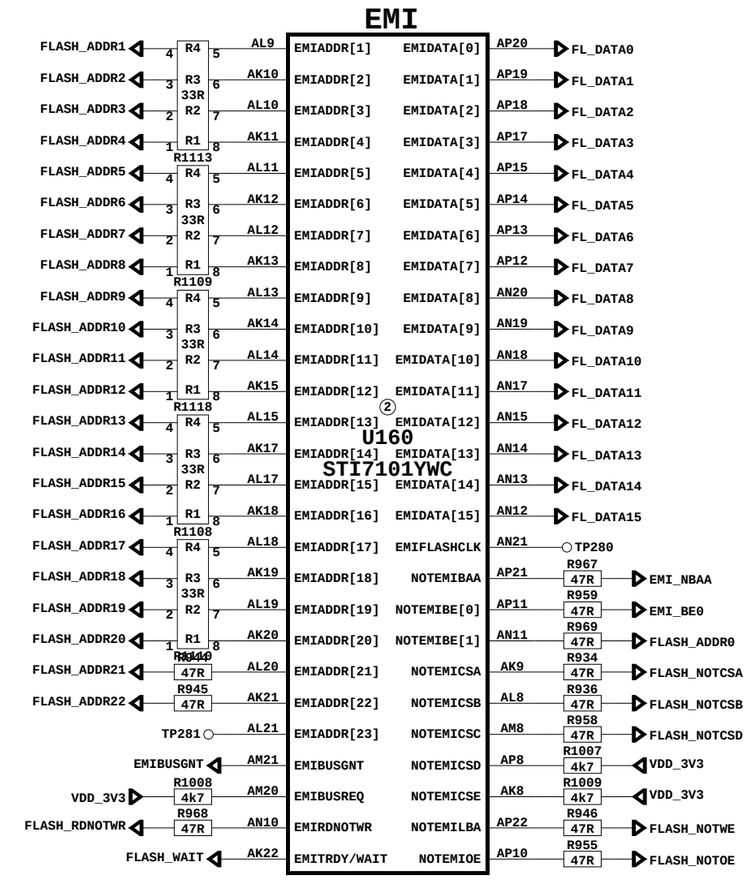


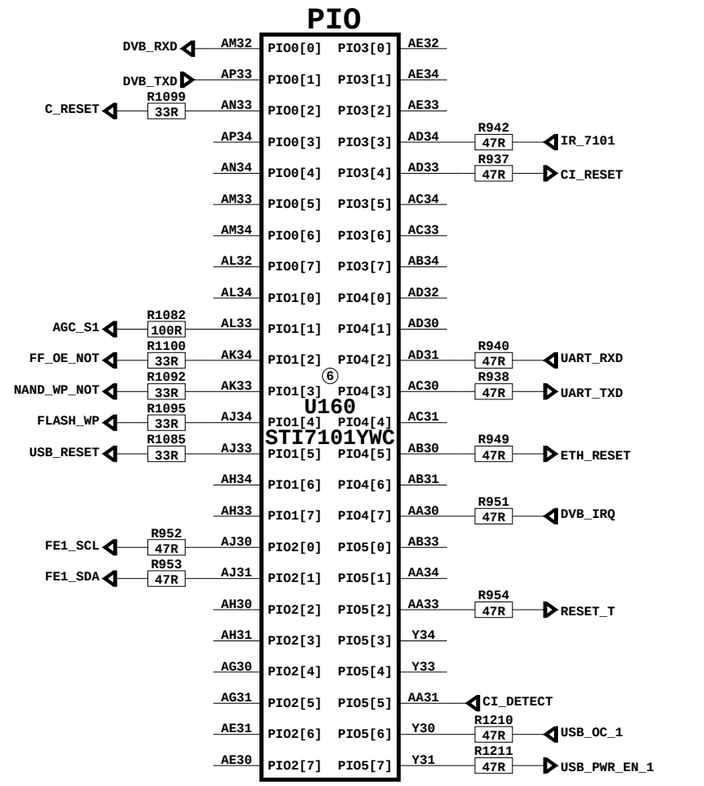


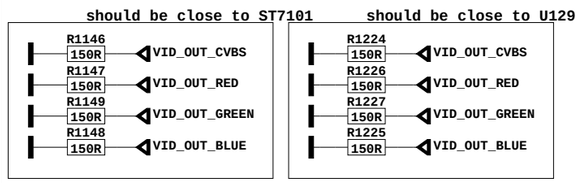


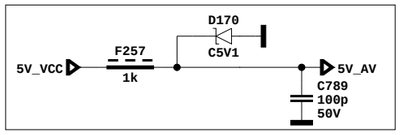
VESTEL	PROJECT NAME : 17mb37	A3
SCH NAME :STi7101 LMI, MISC		SHEET:15OF:18
DRAWN BY :HUSEYIN E. CETIN		14-10-2009_09:10

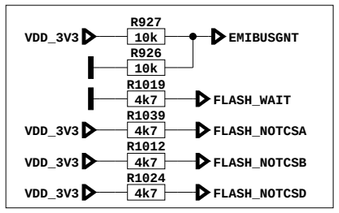


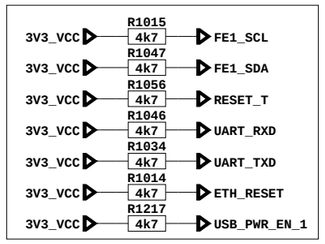


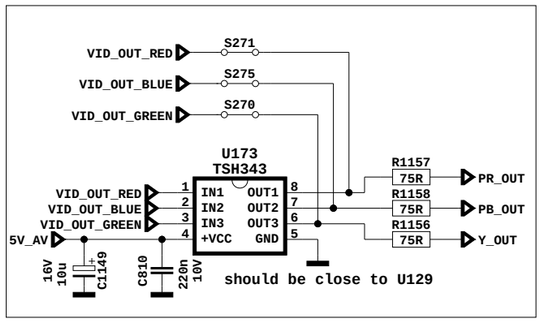


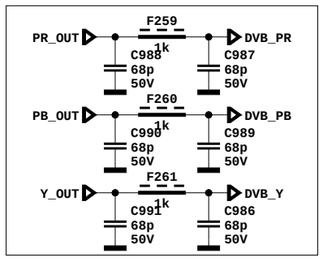


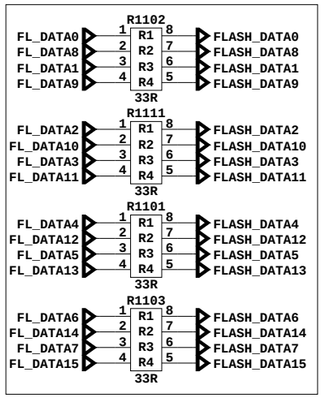


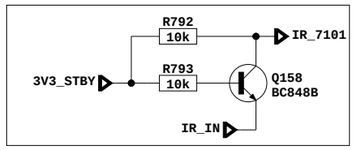


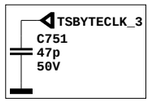


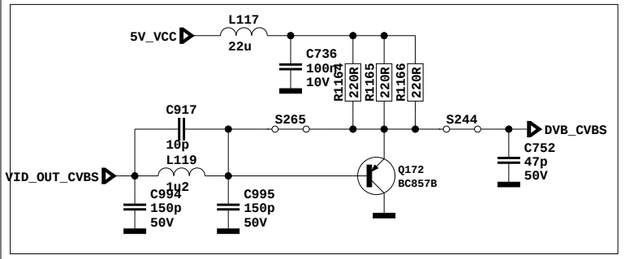


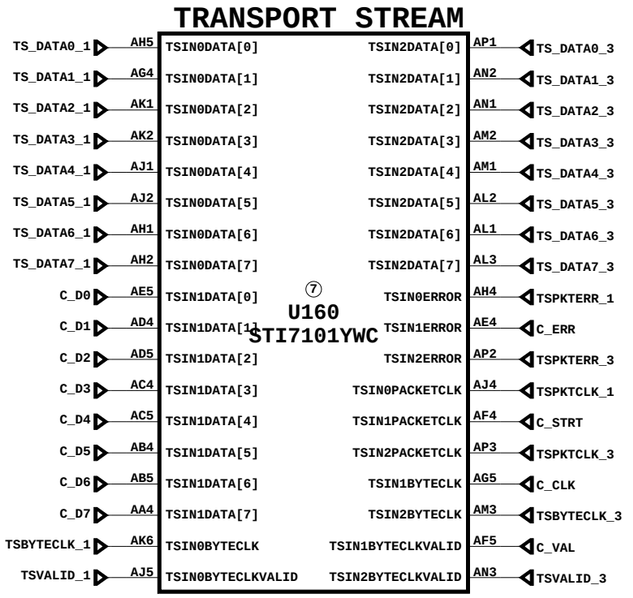




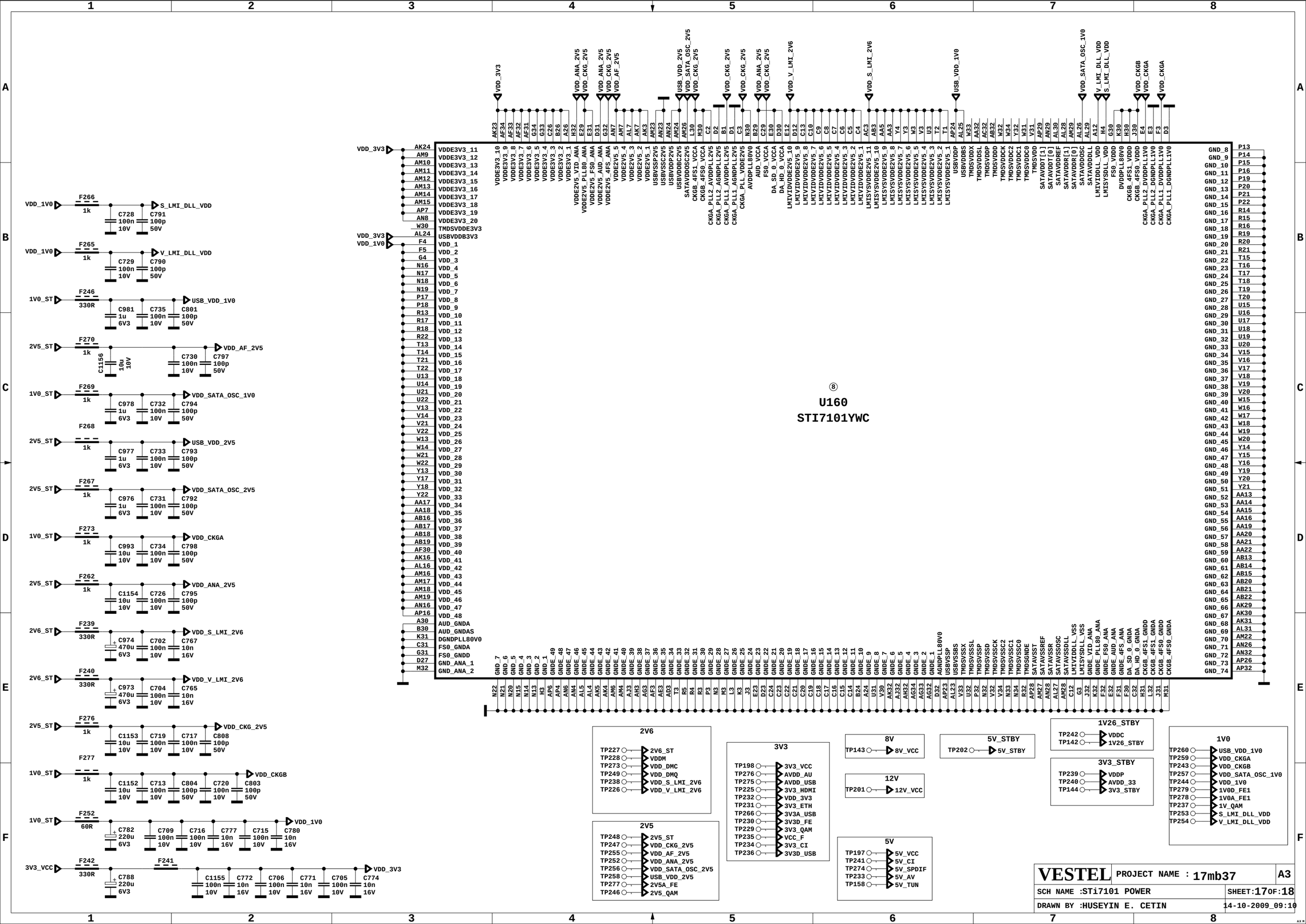


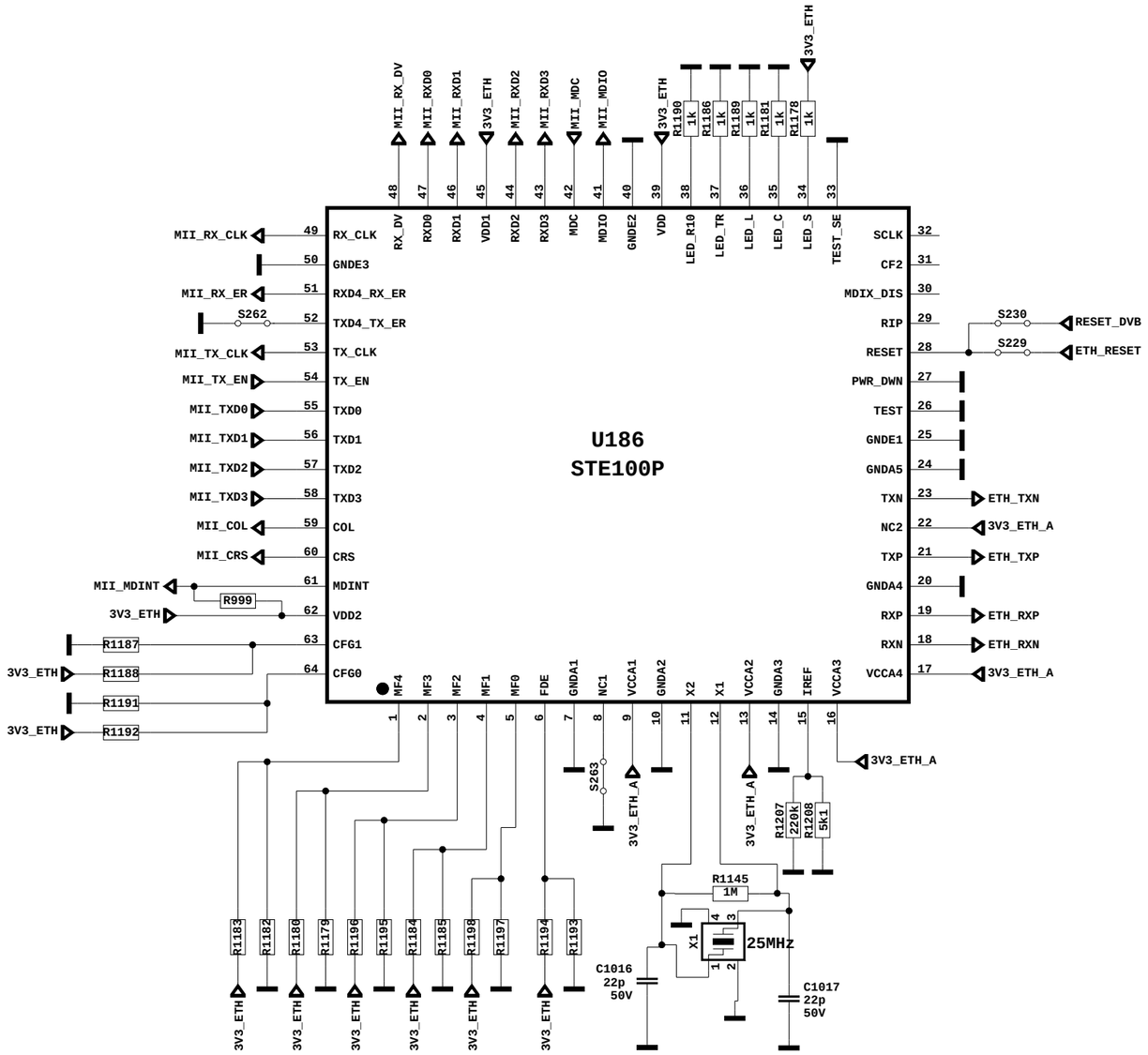


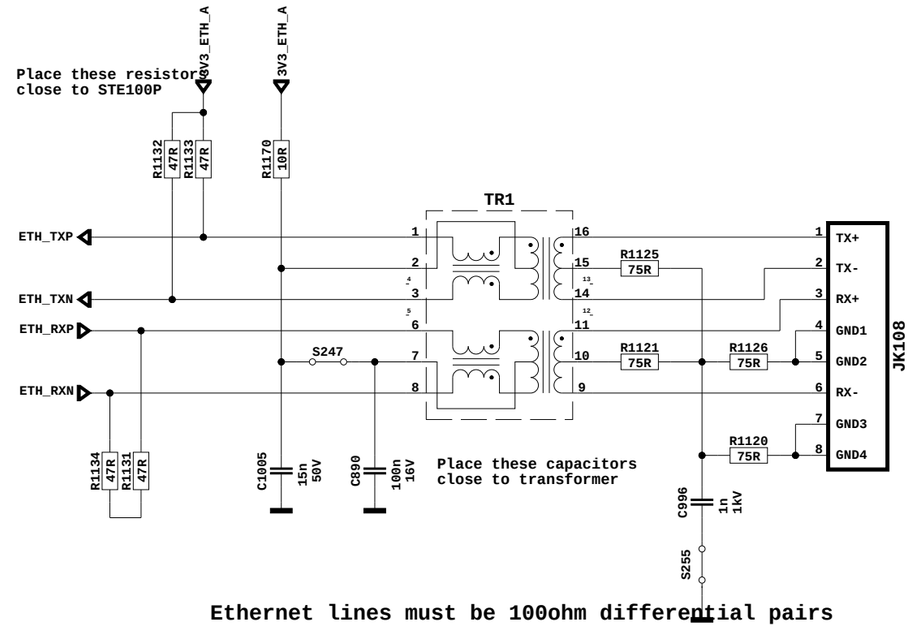




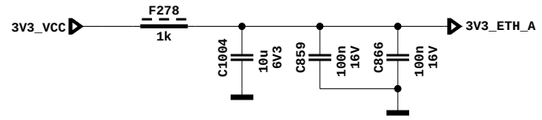
VESTEL	PROJECT NAME : 17mb37	A3
SCH NAME :STi7101 A/V, PIO, EMI, TS	SHEET:16 OF:18	
DRAWN BY :HUSEYIN E. CETIN	14-10-2009_09:10	

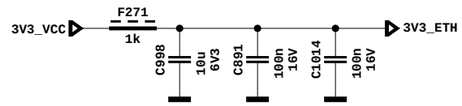

VDD_1V0
F266
1k
C728 100n 10V
C791 100p 50V
S_LMI_DLL_VDD
F265
C729 100n 10V
C790 100p 50V
V_LMI_DLL_VDD
1V0_ST
F246
330R
C981 1u 6V3
C735 100n 10V
C801 100p 50V
USB_VDD_1V0
2V5_ST
F270
C1156 10u 10V
C730 100n 10V
C797 100p 50V
VDD_AF_2V5
F269
C978 1u 6V3
C732 100n 10V
C794 100p 50V
VDD_SATA_OSC_1V0
F268
C977 1u 6V3
C733 100n 10V
C793 100p 50V
USB_VDD_2V5
F267
C976 1u 6V3
C731 100n 10V
C792 100p 50V
VDD_SATA_OSC_2V5
F273
C993 10u 10V
C734 100n 10V
C798 100p 50V
VDD_CKGA
F262
C1154 10u 10V
C726 100n 10V
C795 100p 50V
VDD_ANA_2V5
2V6_ST
F239
330R
C974 470u 6V3
C702 100n 10V
C767 10n 16V
VDD_S_LMI_2V6
F240
C973 470u 6V3
C704 100n 10V
C765 10n 16V
VDD_V_LMI_2V6
F276
C1153 10u 10V
C719 100n 10V
C717 100n 10V
C808 100p 50V
VDD_CKG_2V5
F277
C1152 10u 10V
C713 100n 10V
C804 100p 50V
C720 100n 10V
C803 100p 50V
VDD_CKGB
F252
60R
C782 220u 6V3
C709 100n 10V
C716 100n 10V
C777 10n 16V
C715 100n 10V
C780 10n 16V
VDD_1V0
3V3_VCC
F242
330R
F241
C788 220u 6V3
C1155 100n 10V
C772 10n 16V
C706 100n 10V
C771 10n 16V
C705 100n 10V
C774 10n 16V
VDD_3V3
VDD_3V3 AK24 VDDE3V3_11
AM9 VDDE3V3_12
AM10 VDDE3V3_13
AM11 VDDE3V3_14
AM12 VDDE3V3_15
AM13 VDDE3V3_16
AM14 VDDE3V3_17
AM15 VDDE3V3_18
AP7 VDDE3V3_19
AN8 VDDE3V3_20
W30 TMDSVDDE3V3
VDD_3V3 AL24 USBVDDB3V3
VDD_1V0 F4 VDD_1
F5 VDD_2
G4 VDD_3
N16 VDD_4
N17 VDD_5
N18 VDD_6
N19 VDD_7
P17 VDD_8
P18 VDD_9
R13 VDD_10
R17 VDD_11
R18 VDD_12
R22 VDD_13
T13 VDD_14
T14 VDD_15
T21 VDD_16
T22 VDD_17
U13 VDD_18
U14 VDD_19
U21 VDD_20
U22 VDD_21
V13 VDD_22
V14 VDD_23
V21 VDD_24
V22 VDD_25
W13 VDD_26
W14 VDD_27
W21 VDD_28
W22 VDD_29
Y13 VDD_30
Y17 VDD_31
Y18 VDD_32
Y22 VDD_33
AA17 VDD_34
AA18 VDD_35
AB16 VDD_36
AB17 VDD_37
AB18 VDD_38
AB19 VDD_39
AF30 VDD_40
AK16 VDD_41
AL16 VDD_42
AM16 VDD_43
AM17 VDD_44
AM18 VDD_45
AM19 VDD_46
AN16 VDD_47
AP16 VDD_48
A30 AUD_GNDA
B30 AUD_GNDAS
K31 DGNDPLL80V0
C31 FS0_GNDA
G31 FS0_GNDD
D27 GND_ANA_1
M32 GND_ANA_2
AK23 VDD_3V3 VDDE3V3_10
AF34 VDDE3V3_9
AF33 VDDE3V3_8
AF32 VDDE3V3_7
AF31 VDDE3V3_6
G34 VDDE3V3_5
G33 VDDE3V3_4
C26 VDDE3V3_3
B26 VDDE3V3_2
A26 VDDE3V3_1
H32 VDD_ANA_2V5 VDDE2V5_VID_ANA
E29 VDD_CKG_2V5 VDDE2V5_PLL80_ANA
E31 VDDE2V5_FS0_ANA
D31 VDD_ANA_2V5 VDDE2V5_AUD_ANA
G32 VDD_CKG_2V5 VDDE2V5_4FS_ANA
AM7 VDD_AF_2V5 VDDE2V5_5
AM7 VDDE2V5_4
AL7 VDDE2V5_3
AK7 VDDE2V5_2
AK3 VDDE2V5_1
AM23 USBVSSP2V5
AN23 USBVSSC2V5
AN24 USBVDDP2V5
AM24 USBVDDBC2V5
AM26 USB_VDD_2V5 SATAVDDOSC2V5
L30 VDD_SATA_OSC_2V5 CKGB_4FS1_VCCA
M30 VDD_CKG_2V5 CKGB_4FS0_VCCA
C2 CKGA_PLL2_AVDDPLL2V5
D2 CKGA_PLL2_AGNDPLL2V5
B1 VDD_CKG_2V5 CKGA_PLL1_AVDDPLL2V5
D1 CKGA_PLL1_AGNDPLL2V5
C3 VDD_CKG_2V5 CKGA_PLL_VDDE2V5
N30 AVDDPLL80V0
B29 VDD_ANA_2V5 AUD_VCCA
C29 VDD_CKG_2V5 FS0_VCCA
E30 DA_SD_0_VCCA
D30 DA_HD_0_VCCA
E12 VDD_V_LMI_2V6 LMIVIDVDDE2V5_10
D12 LMIVIDVDDE2V5_9
C13 LMIVIDVDDE2V5_8
C10 LMIVIDVDDE2V5_7
C9 LMIVIDVDDE2V5_6
C8 LMIVIDVDDE2V5_5
C7 LMIVIDVDDE2V5_4
C6 LMIVIDVDDE2V5_3
C5 LMIVIDVDDE2V5_2
C4 LMIVIDVDDE2V5_1
AC3 VDD_S_LMI_2V6 LMISYSVDDE2V5_11
AB3 LMISYSVDDE2V5_10
AA5 LMISYSVDDE2V5_9
AA3 LMISYSVDDE2V5_8
Y4 LMISYSVDDE2V5_7
Y3 LMISYSVDDE2V5_6
W3 LMISYSVDDE2V5_5
V3 LMISYSVDDE2V5_4
U3 LMISYSVDDE2V5_3
T2 LMISYSVDDE2V5_2
T1 LMISYSVDDE2V5_1
AP24 USB_VDD_1V0 USBVDDP
AL25 USBVDDBS
W33 TMDSVDDX
AA32 TMDSVDDSL
AC32 TMDSVDDP
AB32 TMDSVDDD
W32 TMDSVDDCK
W34 TMDSVDDC2
Y32 TMDSVDDC1
W31 TMDSVDDC0
V31 TMDSVDD
AP29 SATAVDDT[1]
AN29 SATAVDDT[0]
AL30 SATAVDDREF
AL28 SATAVDDR[0]
AM29 SATAVDDR[1]
AL26 VDD_SATA_OSC_1V0 SATAVDDOSC
AL29 SATAVDDDLL
A12 V_LMI_DLL_VDD LMIVIDDLL_VDD
H4 S_LMI_DLL_VDD LMISYSDLL_VDD
G30 FS0_VDD
K30 DVDDPLL80V0
H30 CKGB_4FS1_VDDD
J30 CKGB_4FS0_VDDD
E4 VDD_CKGB CKGB_PLL2_DVDDPLL1V0
E3 VDD_CKGA CKGA_PLL2_DGNDPLL1V0
F3 CKGA_PLL1_DVDDPLL1V0
D3 VDD_CKGA CKGA_PLL1_DGNDPLL1V0
GND_8 P13
GND_9 P14
GND_10 P15
GND_11 P16
GND_12 P19
GND_13 P20
GND_14 P21
GND_15 P22
GND_16 R14
GND_17 R15
GND_18 R16
GND_19 R19
GND_20 R20
GND_21 R21
GND_22 T15
GND_23 T16
GND_24 T17
GND_25 T18
GND_26 T19
GND_27 T20
GND_28 U15
GND_29 U16
GND_30 U17
GND_31 U18
GND_32 U19
GND_33 U20
GND_34 V15
GND_35 V16
GND_36 V17
GND_37 V18
GND_38 V19
GND_39 V20
GND_40 W15
GND_41 W16
GND_42 W17
GND_43 W18
GND_44 W19
GND_45 W20
GND_46 Y14
GND_47 Y15
GND_48 Y16
GND_49 Y19
GND_50 Y20
GND_51 Y21
GND_52 AA13
GND_53 AA14
GND_54 AA15
GND_55 AA16
GND_56 AA19
GND_57 AA20
GND_58 AA21
GND_59 AA22
GND_60 AB13
GND_61 AB14
GND_62 AB15
GND_63 AB20
GND_64 AB21
GND_65 AB22
GND_66 AK29
GND_67 AK30
GND_68 AK31
GND_69 AL31
GND_70 AM22
GND_71 AN26
GND_72 AN32
GND_73 AP26
GND_74 AP32
GND_7 N22
GND_6 N21
GND_5 N20
GND_4 N15
GND_3 N14
GND_2 N13
GND_1 H3
GNDE_49 AP6
GNDE_48 AP4
GNDE_47 AN6
GNDE_46 AN4
GNDE_45 AL5
GNDE_44 AL4
GNDE_43 AK5
GNDE_42 AK4
GNDE_41 AM6
GNDE_40 AM4
GNDE_39 AJ3
GNDE_38 AH3
GNDE_37 AG3
GNDE_36 AF3
GNDE_35 AE3
GNDE_34 AD3
GNDE_33 T3
GNDE_32 R5
GNDE_31 R4
GNDE_30 R3
GNDE_29 P3
GNDE_28 N3
GNDE_27 M3
GNDE_26 L3
GNDE_25 K3
GNDE_24 J3
GNDE_23 E23
GNDE_22 D23
GNDE_21 C24
GNDE_20 C23
GNDE_19 C22
GNDE_18 C21
GNDE_17 C20
GNDE_16 C19
GNDE_15 C18
GNDE_14 C17
GNDE_13 C16
GNDE_12 C15
GNDE_11 C14
GNDE_10 B24
GNDE_9 A24
GNDE_8 U31
GNDE_7 V30
GNDE_6 AK32
GNDE_5 AJ32
GNDE_4 AH32
GNDE_3 AG34
GNDE_2 AG33
GNDE_1 AG32
AGNDPLL80V0 D32
USBVSSP AP23
USBVSSBS AL23
TMDSVSSX V33
TMDSVSSSL U32
TMDSVSSP P32
TMDSVSSD N32
TMDSVSSCK V32
TMDSVSSC2 V34
TMDSVSSC1 M33
TMDSVSSC0 N34
TMDSGNDE R32
SATAVSST AP28
SATAVSSREF AM27
SATAVSSR AN28
SATAVSSOSC AL27
SATAVSSDLL AM28
LMIVIDDLL_VSS C12
LMISYSDLL_VSS G3
GNDE_VID_ANA J32
GNDE_PLL80_ANA K32
GNDE_FS0_ANA F32
GNDE_AUD_ANA E32
GNDE_4FS_ANA F31
DA_SD_0_GNDA F30
DA_HD_0_GNDA C32
CKGB_4FS1_GNDD H31
CKGB_4FS1_GNDA L32
CKGB_4FS0_GNDD J31
CKGB_4FS0_GNDA M31
⑧
U160
STI7101YWC
2V6
TP227 2V6_ST
TP228 VDDM
TP273 VDD_DMC
TP249 VDD_DMQ
TP238 VDD_S_LMI_2V6
TP226 VDD_V_LMI_2V6
2V5
TP248 2V5_ST
TP247 VDD_CKG_2V5
TP255 VDD_AF_2V5
TP252 VDD_ANA_2V5
TP256 VDD_SATA_OSC_2V5
TP258 USB_VDD_2V5
TP277 2V5A_FE
TP246 2V5_QAM
3V3
TP198 3V3_VCC
TP276 AVDD_AU
TP275 AVDD_USB
TP225 3V3_HDMI
TP232 VDD_3V3
TP231 3V3_ETH
TP266 3V3A_USB
TP230 3V3D_FE
TP229 3V3_QAM
TP235 VCC_F
TP234 3V3_CI
TP236 3V3D_USB
8V
TP143 8V_VCC
12V
TP201 12V_VCC
5V
TP197 5V_VCC
TP241 5V_CI
TP274 5V_SPDIF
TP233 5V_AV
TP158 5V_TUN
5V_STBY
TP202 5V_STBY
1V26_STBY
TP242 VDDC
TP142 1V26_STBY
3V3_STBY
TP239 VDDP
TP240 AVDD_33
TP144 3V3_STBY
1V0
TP260 USB_VDD_1V0
TP259 VDD_CKGA
TP243 VDD_CKGB
TP257 VDD_SATA_OSC_1V0
TP244 VDD_1V0
TP279 1V0D_FE1
TP278 1V0A_FE1
TP237 1V_QAM
TP253 S_LMI_DLL_VDD
TP254 V_LMI_DLL_VDD
VESTEL
PROJECT NAME : 17mb37
A3
SCH NAME :STi7101 POWER
SHEET:17OF:18
DRAWN BY :HUSEYIN E. CETIN
14-10-2009_09:10





Ethernet lines must be 100ohm differential pairs





VESTEL	PROJECT NAME : 17mb37	A3
SCH NAME :ETHERNET		SHEET:18 OF:18
DRAWN BY :ERTUG BAL		14-10-2009_09:10